Optical Spatial Quantization for Higher Performance Analog-to-Digital Conversion

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Abstract—A novel optical spatial quantized analog-to-digital conversion scheme for real-time conversion at ultrahigh sampling frequencies is presented. At each sampling instant, the analog input voltage deflects an optical sampling pulse onto an array of photodetectors. The output code is derived from the output voltages of the photodetectors on which the optical beam lands. Particular benefits of the proposed architecture are significant reduction in jitter through the use of a mode-locked laser to generate the sampling pulses, high quantization bandwidth through a fully optical quantization scheme, and the system simplicity through the use of just one phase modulator and an embedded binary encoder in the binary-connected photodetector arrays. We experimentally demonstrate an eight-level quantization consuming only 7.2 pJ per quantization with 18-GHz bandwidth, projected to an estimated 8-ps full-width half-maximum (FWHM) photodetector output voltages promise the potential of realizing a 3-bit 125-GS/s analog-to-digital converter.

Index Terms—Analog-to-digital conversion, mode-locked lasers, optical sampling, phase modulation, photodetector.

I. INTRODUCTION

Achieving the high sampling rates required for direct conversion of wideband analog electrical signals to digital remains at the heart of the trend towards maximally digital electronic systems. With rapidly increasing signal bandwidths comes a corresponding need for higher speed analog-to-digital conversion [1], [2]. There has been a tremendous amount of work on analog-to-digital converters (ADCs) operating at gigasamples to tens of gigasamples per second sampling rates, with large input bandwidths and moderate resolutions. This type of high-speed ADC is of particular interest for test and measurement equipment [3]–[6], optical communications [7], and wireless communications such as digital receivers [8], [9] software radio [10], and wideband radar [11].

Optical techniques are believed to have a great potential for realizing high-speed ADCs thanks to the large bandwidth of optical modulators and low-jitter ultra-high-speed sampling clocks offered by mode-locked lasers [12]. Equally significant is the ability to distribute optical clocks without a consequent increase in amplitude and phase noise due to the robust nature of photons for transmitting information. A number of optical analog-to-digital conversion schemes have been proposed to overcome the limited sampling speed of electronic ADCs. Many of the proposed optical ADCs employ optical sampling to overcome the timing jitter limitation of electronic sampling circuits, but use electronic ADCs for quantization [12]–[14]. Optical time-stretch ADCs [15] are based on stretching the signal in time prior to electronic digitization. Another category of optical ADCs employs optical quantization by using optical modulators [16]–[21]. Among this category are the interferometric ADCs, first proposed by Taylor [22], which use an array of phase modulators with geometrically increasing lengths. Although the first generation of these ADCs were not practically feasible due to multiple-modulator mismatches and large device sizes, the follow-up work [23] using one phase modulator with binary encoding shows a great potential for achieving high-speed analog-to-digital conversion.

Here, we analyze the operation of an optical spatial quantized ADC based on the interferometric analog-to-digital conversion scheme (first proposed in [24]). We explain that the proposed architecture not only benefits from the low-jitter high-speed optical sampling clocks and the large bandwidth of the optical phase modulators, but, in contrast to other interferometric techniques, it also takes advantage of a fully differential binary encoder embedded in the binary-connected photodetectors to directly resolve the ADC output bits. We experimentally demonstrate an eight-level quantization consuming only 7.2 pJ per quantization operation over an 18-GHz bandwidth. Measured 8-ps full-width half-maximum (FWHM) photodetector output voltages promise the realization of a 3-bit 125-GS/s ADC with this architecture.

II. OVERVIEW OF THE OPTICAL SPATIAL QUANTIZED ADC

The architecture of the proposed ADC system is shown in Fig. 1. An optical input from a mode-locked laser is first coupled into an input waveguide. The optical pulse then splits and propagates down two waveguide branches as part of a Mach–Zehnder interferometer. A phase modulator is integrated in one of the branches to vary the phase of the optical pulses according to the analog electrical signal to be digitized. A fully differential implementation could be achieved by applying a differential signal to both branches. After passing through the half Mach–Zehnder interferometer, the optical beams from the two
branches enter a slab waveguide region, which allows free propagation in the lateral direction and then diverge and interfere. The resulting interference pattern from the two optical pulses forms a spot on an effective image plane, a spot whose position is proportional to the phase difference between the two optical pulses. In effect, the combination of the phase modulator and the free-propagation region together constitute an imaging beam-deflection system whose deflection is determined by the phase difference between the two optical pulses entering the free-propagation region and, more specifically, by the modulating electrical signal.

Integrating photodetector arrays inside the output waveguides at appropriate positions along the image plane enables measurement of the spatial distribution of optical power. Therefore, the number of output waveguides determines the total number of resolvable quantization levels. The ADC output quantization levels, specified by $V_{\text{th}}^{\text{out}}(j = 1, 2, \ldots, b)$, are resolved by connecting the photodetector arrays in a binary fashion, where $b$ is the ADC resolution.

Using the 2-D beam propagation simulation package BEAM-PROP [25], we modeled the optical intensity variations on the image plane as a function of the modulator phase shift provided by the analog electronic signal. Simulation results, illustrated in Fig. 2, show a $\pm 6^\circ$ deflection angle of the resulting interference pattern within the $2\pi$ phase shift, while using a 700-$\mu$m-wide 350-$\mu$m-long free propagation region.

We use Fraunhofer diffraction theory to further analyze the beam-deflection operation in the discussed architecture. According to Fraunhofer diffraction theory [26], the optical pattern on the image plane would be the Fourier transform of the optical pattern entering the free propagation region scaled by a $\lambda \cdot L$ factor. This theory is valid if the image plane is in the far field of the two optical beams entering the free propagation region

$$d^2 \ll \lambda \cdot L$$  \hspace{1cm} (1)

where $\lambda$ is the optical wavelength, $L$ is the length of the free propagation region, and $d$ is the spacing between two input waveguides. The intensity of the resulting optical pattern on the image plane is calculated as

$$I = \frac{1}{w_0} \frac{d}{\lambda L} P_0 \sin^2 \left( \frac{x d}{\lambda L} \right) \left( 1 + \cos \left( \frac{2\pi x d}{\lambda L} \right) - \Delta \phi \right)$$  \hspace{1cm} (2)

where $\Delta \phi$ is the phase shift induced by the phase modulator, $w_0$ is the optical mode size in the input waveguide (assuming a circular optical mode shape), $P_0$ is the optical clock power, and $x$ is the position on the image plane. The resulting optical peak on the image plane (Fig. 3) is deflected uniformly by $\pm (L\lambda/2d)$ over an induced phase shift of $\pm \pi$.

In order to resolve $b$ output bits, the full deflection range on the image plane is divided between $N$ output waveguides, where $N = 2^b$. The optical power coupled to the $i$th output waveguide is given by

$$P_i \approx \frac{1}{N} P_0 \sin^2 \left( \frac{x_i d}{\lambda L} \right) \left( 1 + \cos \left( \frac{2\pi x_i d}{\lambda L} \right) - \Delta \phi \right)$$  \hspace{1cm} (3)
where

\[ x_i = \left( i - \frac{N + 1}{2} \right) \frac{\lambda L}{dN}, \quad i = 1, 2, \ldots, N. \]

Since the photodetector arrays integrated in the output waveguides are connected in a binary fashion, the differential output voltage representing the \( j \)th output bit, \( V_{\text{bit}}^{(j)} \), is calculated as

\[ V_{\text{bit}}^{(j)} = \sum_{i=1}^{i=N} (-1)^{b_{i-1}} S(P_i) \cdot P_i \cdot R \cdot \left( 1 - e^{-\frac{t}{\tau}} \right) \quad (4) \]

where \( S \) is the photodetector responsivity, \( R \) is the photodetector resistance, \( t \) is half of the clock period, and \( \tau \) is the \( RC \) time constant of the photodetector.

The resulting voltage for each output bit would be a sinusoidal signal. By linear photodetectors, we cannot get more than one period of the sinusoidal signal per \( 2\pi \) phase modulation. However, by employing nonlinear photodetectors, it would be possible to get a periodic output voltage with up to \( 2^{b-1} \) periods per \( 2\pi \) phase modulation for the \( j \)th output bit. Therefore, the binary-connected nonlinear photodetectors can also perform the binary encoding (positive and negative output voltages represent digital “1” and “0,” respectively).

By employing this encoding technique, we can increase the ADC resolution without having to use a large number of phase modulators or photodetectors. By accurately designing the photodetector arrays and their nonlinearity, it would also be possible to get more square (rather than sinusoidal) output bit voltages over the induced phase modulation. Moreover, the differential encoding scheme implies a small sensitivity of the ADC output to the laser power fluctuations. In this study, we operate the photodetectors in the saturation regime to take advantage of their nonlinear characteristics.

III. OPTICAL SPATIAL QUANTIZED ADC PERFORMANCE

The bandwidth of the optical spatial quantized ADC is determined by the bandwidth of the beam deflector, or more specifically, by the phase modulator bandwidth. The optical phase shift introduced by a traveling-wave phase modulator is given by

\[ \Delta \phi = \chi V_{\text{in}} L_m \frac{1-e^{-\alpha(f)L_m}}{\alpha(f)L_m} (1-e^{-t/T_{\text{sett}}}) \quad (5) \]

where \( \chi \) is the phase modulation efficiency in degrees \( V^{-1} \) mm\(^{-1} \), \( V_{\text{in}} \) is the modulating electric voltage, \( L_m \) is the length of the modulator, \( T_{\text{sett}} \) is the phase settling time of the modulator, and \( \alpha(f) \) is the microwave attenuation.

In order to keep the maximum ADC error to 0.5 LSB

\[ \text{Max} \Delta \phi_{\text{error}} \leq \frac{1}{2} \Delta \phi_{\text{LSB}} \quad (6) \]

where \( \Delta \phi_{\text{error}} \) is the phase shift deviation from ideal case (no microwave loss and speed limitation), and \( \Delta \phi_{\text{LSB}} \) is the required phase shift for resolving the LSB bit. Therefore,

\[ 2\pi \left( 1 - \frac{1-e^{-\alpha(f)L_m}}{\alpha(f)L_m} \right) \left( 1 - e^{-t/T_{\text{sett}} \text{[deg]}} \right) \leq \frac{1}{2} \frac{2\pi}{2^}\text{LSB}. \quad (7) \]

For a Nyquist rate ADC, (7) should be evaluated for \( t = 1/f_s \) \( (f_s = 2B_W) \), where \( f_s \) and \( B_W \) are the ADC sampling frequency and bandwidth, respectively.

The computed ADC bandwidth will diminish further when microwave loss of the phase modulating electrical signal are included. Skin effect and field coupling to the substrate increase the microwave loss dramatically at high frequencies [27]. The collective effect of all such loss mechanisms ultimately bounds the useful operational bandwidth for a desired ADC resolution. The effect of microwave loss can be reduced by increasing the phase modulation efficiency to allow the use of a shorter phase modulator.

As modulation techniques keep improving, higher phase modulation efficiencies and smaller phase modulation settling times are achieved. State-of-the-art phase modulation settling times can be on the order of few picoseconds, making it possible to achieve high conversion bandwidths through this architecture.

Equation (8) shows the tradeoff between the ADC resolution and bandwidth using the optical spatial quantized scheme. Other ADC resolution limiting factors are phase modulator nonlinearity, photodetector mismatches, waveguide misalignments, and crosstalk between the output waveguide channels.

Noise is another important factor limiting the ADC resolution. The noise sources contributing to the signal-to-noise ratio degradation in the optical spatial quantized ADC are the optical shot noise in output photodetectors, thermal noise in the termination resistance and output photodetectors, and a background noise resulting from optical reflections at device boundaries. It should be mentioned that the mode-locked laser noise effect is neglected, due to the fully differential detection architecture.

In contrast to conventional ADC schemes, the optical clock power directly affects the ADC output voltages in the optical spatial quantized scheme (3), (4). This indicates a great potential for increasing the ADC signal-to-noise ratio, and ADC resolution, by increasing the optical clock power.

IV. PHASE MODULATOR DESIGN AND MEASUREMENT RESULTS

The phase modulation mechanism is based on the quantum-confined Stark effect, in which an applied perpendicular electric field induces a shift in the absorption spectrum, and an accompanying shift in the refractive index of a multiple quantum well structure [28].

In this study, multiple quantum well layers are designed as integral parts of the intrinsic region of a p-i-n diode integrated inside the optical waveguide, which is designed for single transverse mode operation for wavelengths longer than 860 nm. The phase-modulating electric signal, which in combination with the substrate bias generates the electric field across the multiple quantum well layers, propagates on a coplanar waveguide...
GaAs layer on a semiinsulating GaAs substrate. The 2-, and remains within a 6% and admittance per unit length. The line impedance per unit length is characterized by a conventional CPW inductance and resistance per unit length. The line parallel-plate capacitance and the waveguide diode depletion region capacitance (operated in reverse bias), together with a series resistance modeling the semiconductor losses associated with transverse current flow, represent the line admittance per unit length. The 50-Ω CPW termination is fabricated using a part of the waveguide semiconductor.

The phase settling time of the modulator \( T_{\text{settling}} \) is given by

\[
T_{\text{settling}} = 2.2 \frac{d_m}{V} + 2\pi \frac{\rho C}{d_m} + 2\pi L_m \frac{V_0 - V_c}{V_c} \tag{9}
\]

where \( d_m \) is the depletion region depth, \( L_m \) is the length of the phase modulator, \( V \) is the carrier average drift velocity across the depletion region, \( \rho \) is the p-i-n diode contact resistivity, and \( V_0 \) and \( V_c \) are the velocities of the optical wave and the microwave, respectively.

CPW scattering parameters of a 1-mm-long phase modulator and the extracted characteristic impedance and propagation constant are shown in Fig. 5. The extracted characteristic impedance is quite close to 50 Ω, and remains within a 6% deviation throughout the measurement range. This impedance level allows the modulator input/output to be connected easily to conventional 50-Ω RF systems. The satisfactory agreement between the experimental microwave velocity and the desired optical velocity of 0.31\( c \) (\( c = 3 \times 10^8 \) m/s) assures less than a 2% microwave-optical velocity mismatch for frequencies below 50 GHz. The experimental RF attenuation is also shown in Fig. 5. The device performance can be improved by increasing the center strip width to reduce attenuation caused by metal microwave loss.

By calculating the CPW propagation constant from scattering parameter measurements as a function of frequency, an electric field settling time of 2.1 ps is estimated for a 1.5-mm-long phase modulator. The expected operational bandwidth of the quantization system utilizing this phase modulator is 30 GHz, where the microwave attenuation of the CPW is the primary bandwidth-limiting mechanism.

Fig. 6 shows the measured phase modulation characteristics at 870-nm wavelength. A relatively linear phase change of 270° V \(-1\) mm \(^{-1}\) and an optical loss of less than 0.28 dB V \(-1\) mm \(^{-1}\) are measured at 2.1-V reverse bias voltage. Using a 1.5-mm active region phase modulator, we measured a 2\(\pi\) phase shift over a ±450-mV analog input signal voltage range.

**V. PHOTODETECTOR DESIGN AND MEASUREMENT RESULTS**

Each photodetector comprises p-i-n diodes monolithically fabricated along the output waveguides. It consists of an active region terminated in 50 Ω through 6-μm metal spacing on either side. The generated photocurrent along the active region is a function of the multiple quantum well reverse bias set by the substrate voltage. The simulation results suggest an optical
absorption coefficient of 1.5 mm\(^{-1}\) along the photodetector under 6-V reverse bias. The combination of the 0.218-fF/\(\mu\)m parasitic capacitance along the photodetector and the 50-\(\Omega\) termination resistance implies an FWHM output pulse width of 5.5 ps for a 400-\(\mu\)m photodetector.

The response of the 400-\(\mu\)m photodetector to a 150-fs input pulse is 8-ps FWHM at 6-V reverse bias [see Fig. 7(a)]. This indicates the capability of the photodetector to detect an optical pulse train at 125 GHz. The side peak in the photodetector response in Fig. 7(a) is due to multiple reflections in the free propagation region and the output waveguide boundaries, degrading the ADC signal-to-noise ratio at high sampling rates. These reflections can be prevented by covering the structure with an antireflection coating such as a silicon–nitride film.

The responsivity of the 400-\(\mu\)m photodetector is calculated by measuring the photodetector output voltage versus the incident optical pulse energy [see Fig. 7(b)]. While the photodetector saturates at an incident pulse energy of 330 fJ, a responsivity of 3.2 \(\times\) 10\(^{-5}\) A/W is calculated at small incident pulse energy levels. As mentioned before, the photodetectors are operated around the nonlinear (saturation) regime in order to achieve a binary encoding through the binary-connected photodetector arrays.

VI. EXPERIMENTAL RESULTS ON THE FABRICATED ADC

A die micrograph of the fabricated ADC is shown in Fig. 8(a). The phase modulator is 1.5-mm long and the free propagation region is 350-\(\mu\)m long. Lengths of 50, 150, and 400 \(\mu\)m are chosen for the first, second, and third bit photodetector arrays, respectively. Different photodetector lengths are to compensate for the voltage amplitude reduction at higher bit levels. The 150-fs optical sampling pulses from a Ti-sapphire mode-locked laser operating at 870 nm are coupled into the input waveguide by using a lensed fiber and fiber collimators.

The location of the output optical peak is determined by monitoring the output voltage of the arrayed photodetectors. Since the output photodetectors are connected in a binary fashion, the ADC digital output code will be determined according to the polarity of \(V_{\text{bit}1}\), \(V_{\text{bit}2}\), and \(V_{\text{bit}3}\) voltages. The resolved photodetector outputs and the resolved quantization levels within \(\pm 100\)-mV analog input voltage range and an input energy of 2 pJ per optical pulse are shown in Fig. 8(b). By accurately designing the photodetector arrays and their nonlinearity, we would be able to achieve output voltages with steeper zero-
crossings (closer to a square shape rather than a sinusoidal). Depending on the digital technology, we can adjust the optical pulse energy or utilize high gain stages prior to digital circuits to match the output voltage with the technology logic levels.

The linearity of the ADC is characterized by measuring the differential nonlinearity and integral nonlinearity during dc operation of the ADC. The static nonlinearity error of less than 0.2 LSB is calculated [see Fig. 9(a)]. The main source of nonlinearity is the interferometric quantization technique and the phase modulation nonlinearity with respect to the modulating voltage. In addition, optical loss in the phase modulator branch and all other sources of mismatch between the two arms of the half Mach–Zehnder interferometer increase nonlinearity.

To verify the quantization operation, the output voltage to a 10- and 30-MHz analog signal is observed in the time domain at a mode-locked laser sampling clock frequency of \( f_s = 80 \) MHz. The signal-to-noise plus distortion ratio (SNDR) is calculated using the corresponding spectral response [see Fig. 9(b)]. An SNDR of 17.8 and 18.5 dB is obtained for an input signal frequency of \( f_{in} = 10 \) MHz and \( f_{in} = 30 \) MHz, respectively, which confirms an eight-level quantization operation at the subsequent frequencies. The limited repetition rate of the available mode-locked laser prevented measuring SNDR at higher sampling rates. Due to this limitation, we used a new technique for measuring the ADC bandwidth.

The ADC bandwidth is determined by measuring the cutoff frequency at which the ADC error exceeds 0.5 LSB. For this measurement, we monitor the ADC least significant bit output to a 0.9-Vpeak sinusoidal analog input voltage under laser continuous-wave operation. The expected output voltage \( V_{1\text{at3}} \) and its subsequent frequency response at low frequencies and cutoff frequency are shown in Fig. 10(a) and (b). Cutoff frequency can be calculated by comparing the measured frequency response of \( V_{1\text{at3}} \) with theoretical expectations. The measured frequency response of \( V_{1\text{at3}} \) at the analog input frequency of 1 GHz is shown in Fig. 10(c). The response of \( V_{1\text{at3}} \) was satisfactory up to an input signal frequency of 18 GHz, which was the upper frequency limit of the employed spectrum analyzer.

This implies an ADC bandwidth of at least 18 GHz, projected to an estimated bandwidth of 30 GHz.

Fig. 11 compares the number of quantized levels versus the potential sampling frequency of the spatially quantized ADC prototype with other high-speed ADCs, mostly with flash, folded-flash, pipelined, and time-interleaved architectures. The ADCs in the survey are from over 220 converters reported at the IEEE Very Large Scale Integration (VLSI) Circuits Symposium and the IEEE International Solid-State Circuit Conference, as well as in the IEEE Journal of Solid-State Circuits from 1997 to 2007.

Power consumption of the ADC is investigated by looking at the quantization and sampling power consumptions separately. The spatial quantization power is supplied by the input analog signal performing the phase modulation within the \( \pm 0.45 \)-V voltage range, corresponding to 4-mW maximum analog input power, eliminating any static power consumption. As mentioned, the optical pulses from the mode-locked laser not only provide the low jitter sampling clock, but are also recycled in the spatial quantizer to resolve the output bits. As a result, the input optical pulse power directly affects the amplitude of the resolved bits and the quantization resolution. The total energy, including optical power for quantization operation and electrical power dissipation in the photodetectors, is 7.2 pJ per
quantization operation. It should be remembered that the calculated energy consumption of 7.2 pJ per quantization operation does not include the power consumption of the comparator stages, which might be required to generate the standard digital output voltages.

VII. CONCLUSION

Optical spatial quantized analog-to-digital conversion is a promising scheme, which, in contrast to conventional ADCs, eliminates any intermediate sample-and-hold and quantization circuits by directly launching the optical sampling pulses at spatial positions corresponding to quantization levels, and which operates at a frequency limited by the mode-locked laser repetition rate. Particular benefits of the proposed architecture are significant reduction in jitter through the use of a mode-locked laser to generate the sampling pulses, high quantization bandwidth through a fully optical quantization scheme, and lower power consumption by extracting some portions of the required power from the analog electrical signal and optical clock directly.

The experimental results of the optical spatial quantized ADC prototype demonstrate an eight-level quantization consuming only 7.2 pJ per quantization with 18-GHz bandwidth, projected to an estimated bandwidth of 30 GHz. Measured 8-ps FWHM photodetector output voltages promise the potential of realizing a 3-bit 125-GS/s ADC. Current design requires additional comparator stages to resolve the ADC output bits with the technology logic levels. However, the system has the potential of achieving logic level outputs directly by accurately setting the photodetector nonlinearity in the embedded binary encoder.

This technique is of particular value for increasing the flexibility and capability of electronic systems by eliminating many performance-limiting components along the path to the digital domain. Realization of some electronic systems, such as the software radio, may become possible by utilizing such an analog-to-digital conversion technique.

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REFERENCES

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