C-band side-entry Ge quantum-well electroabsorption modulator on SOI operating at 1 V swing

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An electroabsorption modulator using a side-entry architecture achieved a contrast ratio exceeding 3 dB over a 3.5 nm range in the C-band, using a voltage swing of 1 V and operating at 100°C. Modulation was due to the quantum-confined Stark effect from ten Ge/SiGe quantum wells epitaxially grown on silicon-on-insulator (SOI) wafers. The device exploits an asymmetric Fabry-Perot resonator formed between the totally internally reflecting air-SiGe interface and a frustrated total internal reflection from the buried oxide layer of the SOI substrate.

Introduction: Development of photonics based on CMOS-compatible materials and processing may lead to inexpensive optoelectronic components and monolithic integration of photonics and electronics for optical interconnects and networks. The lack of physical mechanisms for light emission or optoelectronic modulation in silicon [1] comparable to those in III–V semiconductors has, however, held back silicon-based optics. Recently we discovered a strong quantum-confined Stark effect (QCSE) in Ge quantum wells with SiGe barriers grown on Si substrates, and demonstrated changes in absorption coefficient similar to those used for high-performance III–V modulators [2, 3]. We also recently demonstrated the first modulator device using this effect [4]. The strong QCSE electroabsorption allowed a novel structure without a waveguide and with very relaxed optical alignment tolerance. The ~10 V required voltage swing was, however, too high for CMOS electronics, and the device did not operate at the important telecommunications C-band wavelengths.

In this Letter, we show a CMOS-compatible 1 V drive, with C-band operation, using a novel frustrated total internal reflection structure. This device retains the alignment tolerance of the previous structure, and demonstrates the compatibility of such modulators with growth on silicon-on-insulator (SOI) substrates, which are often preferred also for other silicon photonics devices.

Our previous Ge/SiGe quantum well QCSE modulator [4] used optical entry and exit ports through the polished edges of the substrate, and light was obliquely incident upon a diode mesa containing quantum wells. Oblique incidence led to the formation of an asymmetric Fabry-Perot resonator owing to total internal reflection (TIR) at the epitaxy/air interface and ~18% reflection at the substrate/epitaxy interface. The lattice mismatch between Si and Ge makes it difficult to grow epitaxial layers of sufficient index contrast and thickness to make distributed Bragg reflectors, and the ~18% reflectivity of the Si-SiGe interface cannot be increased much further by increasing the incident angle without making the focal spot projection on the diode mesa prohibitively large.

In this Letter we report a side-entry modulator fabricated on an SOI wafer with ten epitaxially grown Ge/SiGe quantum wells. Oblique incidence on the buried oxide layer (BOX) leads to frustrated total internal reflection [5]. Choosing the thickness of a low-index layer contained between two high-index layers allows control of the resulting reflectivity. The 50 nm BOX used has ~70% reflectivity at the design angle, increasing the quality factor of the resonator compared to the previous work, reducing the required number of quantum wells and consequently the operating voltage. SOI waveguides typically use a ~1 μm BOX. The thin 50 nm BOX used here is attractive for potential integration of modulators with high-performance electronics, the primary application of SOI wafers.

Experiment and results: The structure starts with an SOI substrate, with a 730 μm-thick Si substrate, followed by the 50 nm BOX and a 100 nm-thick silicon layer. The epitaxial structure grown on this had a 900 nm-thick *p*-type $Si_{0.1}Ge_{0.9}$ layer B-doped at 3×10^{17} cm^{-3}, a 100 nm-thick undoped $Si_{0.1}Ge_{0.9}$ layer, ten Ge quantum wells ~15 nm thick separated by $Si_{0.84}Ge_{0.16}$ barriers ~33 nm thick (all undoped), another 100 nm-thick undoped $Si_{0.1}Ge_{0.9}$ layer, and a top *n*-type $Si_{0.1}Ge_{0.9}$ layer As-doped at 10^{18} cm^{-3}. Growth techniques were similar to our previous work [4]. For optical calculations, we presumed refractive indices of 3.53 for the Si layers, 1.53 for the BOX layer, and 4.15 for the SiGe layers and the quantum-well region.

The effective absorption coefficient spectrum (i.e. using the total thickness of the wells and barriers as the effective absorbing length) of the quantum well superlattice at 100°C, shown in Fig. 1, was calculated from photocurrent measurements made with incident light perpendicular to the surface of an antireflection coated diode mesa. The absorption spectrum was previously found to linearly shift by 0.83 nm/°C [3], so operation at such temperatures can both shift the optical absorption to allow modulation in the C-band and match the operating surface temperatures of high-performance CMOS chips.

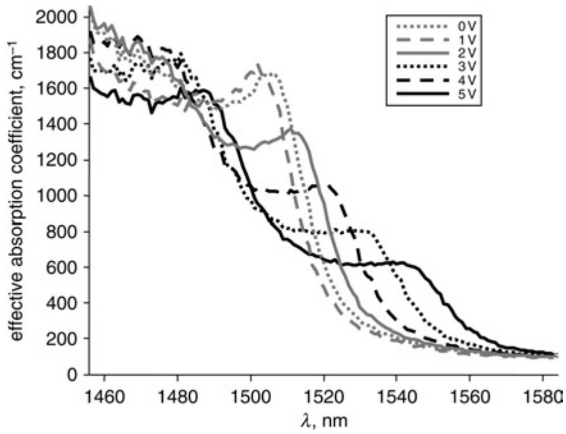

Fig. 1 *Effective absorption coefficient of quantum well superlattice at 100°C with applied reverse bias*

To create side-entry modulators (see the schematic in Fig. 2), 225 × 625 μm rectangular mesas were etched, Cr/Au contacts were deposited, and the parallel edges of the wafer were polished to create a 3.5 mm-wide chip containing a one-dimensional array of modulators.

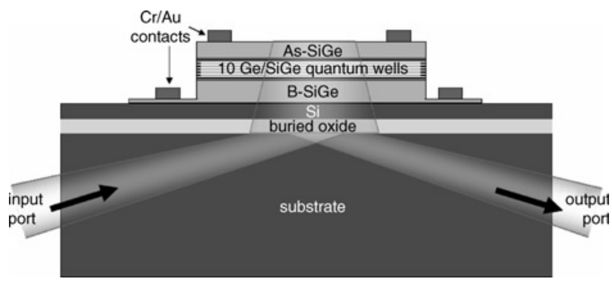

Fig. 2 *Schematic of SOI side-entry modulator (not to scale)*

A Gaussian beam, polarised in the plane of the grown layers, entered the polished edge facet from a 45° angle in air, consequently reaching the bottom of the diode mesa at a 78° oblique angle. (This device operates only in this polarisation – both the optical arrangement and the electroabsorption in the quantum wells are strongly polarisation sensitive.) The beam was focused at the diode mesa, forming an ellipse with minor and major axes of 70 and 484 μm. Transmission through the wafer was measured for wavelength increments of 0.5 nm and voltage increments of 0.125 V. Fig. 3 shows the contrast ratio for voltage swings of 1, 2 and 4 V. A bias voltage (optimised independently for each point in Fig. 3), is required to shift the excitonic absorption peak from its position at 1502 nm for 0 V bias to the longer wavelengths for C-band operation.

For 1 V swing, the contrast ratio exceeds 3 dB from 1539 to 1542.5 nm, and the voltage swing at the contrast ratio peak was from 3.625 to 4.625 V. For 4 V swing, the contrast ratio exceeded 3 dB from 1536 to 1545 nm, and the peak contrast ratio was 6 dB at 1541 nm for a voltage swing from 0.875 to 4.875 V. The transmission at the peak of contrast was 11% with the modulator in the low-absorption state, and it is estimated that, if the entry and exit facets were antireflection coated, the transmission would reach 32%.

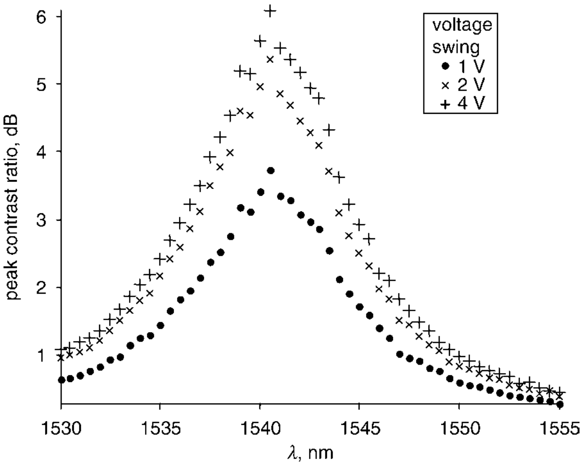

Fig. 3 *Modulator's peak contrast ratio against wavelength*

For 1 V swing at 1541 nm, the contrast ratio exceed 3 dB as the input beam was translated over a distance of 51 and 32 μm for horizontal translations parallel and normal to the edge facet, respectively. The misalignment tolerance greatly exceeds that of waveguide devices. With this relatively large mesa, the device capacitance is estimated to be 33 pF. Smaller mesas, with corresponding reduced misalignment tolerance would, however, allow smaller capacitances, at least to a few picofarads. Simultaneous optimisation of the focal spot size and mesa size, which would affect the contrast ratio, misalignment tolerance, and capacitance, could allow substantially reduced capacitance if desired for high-speed applications. With capacitance at these scales, the device could be useful for small numbers of optical outputs from chips, where the relaxed alignment tolerance of these devices could substantially simplify optical packaging.

Conclusions: The electroabsorption modulator presented here operates in the C-band, with voltage swings compatible with CMOS electronics, without precise spatial alignment or narrow optical resonances, using a fabrication process expected to be compatible with CMOS fabrication, and may be useful for developing a platform to integrate CMOS, short distance optical interconnects, and fibre-based optical networks.

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