

Rise-time Measurements of Low Capacitance CMOS Detectors Using a Pump-Probe Technique

Salman Latif, Sukru Ekin Kocabas, Liang Tang, and David A. B. Miller

Department of Electrical Engineering, Ginzton Laboratory, Stanford University, Stanford, CA, USA

E-mail address: slatif@stanford.edu

Abstract: Optical interconnect and clocking applications require low capacitance, high speed, CMOS-compatible photodetectors. We characterize the small-signal pump-probe response of Silicon on Sapphire CMOS compatible detectors showing response ~ 35 ps.

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Low capacitance, CMOS-compatible photodetectors are a vital component for short range interconnect or on-chip optical timing schemes [1]. We have designed and tested lateral P-I-N detectors in a commercial CMOS process. Figure 1 (a) shows the schematic of the detector structure. The chip has been fabricated in a Silicon-on-Sapphire (SOS) process which uses a 70nm thin layer of silicon as the active layer. Previous work in our group showed that the SOS process was a feasible platform for integrating photodetectors with CMOS electronics, and measured the large signal rise-time of a $6.2 \mu\text{m}$ finger-spacing detector [2]. We now test the integration of these detectors with CMOS circuitry, including also new designs with a minimum finger-spacing of $1.2 \mu\text{m}$ that should enable 10-20 GHz bandwidth operation. To characterize the detectors fully, we have measured the small-signal time response of detectors with four different finger-spacings using optical pump-probe measurements with integrated modulators. This technique allows high-sensitivity small-signal measurements with excellent time resolution, and we observe response as fast as ~ 35 ps, close to the theoretically predicted time response.

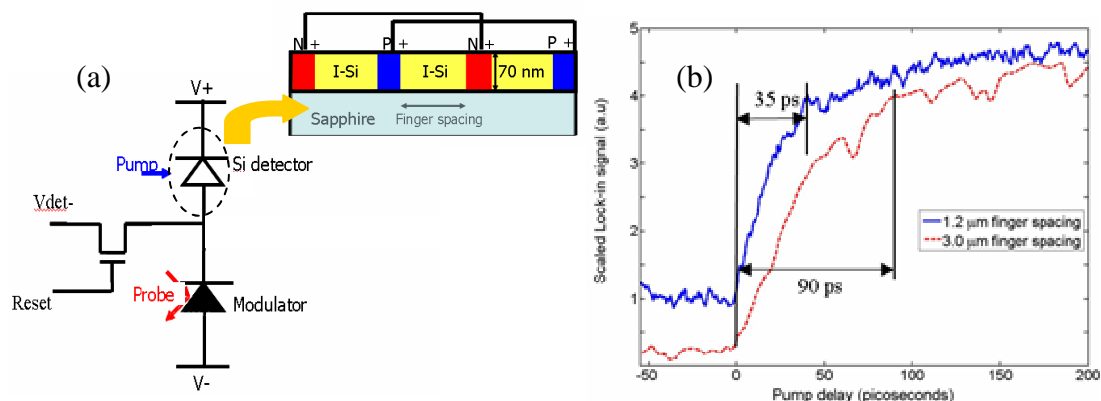


Figure 1: (a) Photodetector speed test -- schematic of the structure under test, showing device connectivity (b) transient response for $1.2 \mu\text{m}$ (solid) and $3.0 \mu\text{m}$ (dashed) finger spacing detectors

Figure 1(a) gives the test schematic. The pump-probe technique relies on the presence of Multiple Quantum Well (MQW) GaAs modulators on chip (connected to various nodes on the chip via hybrid integration techniques), whose reflectivity, which varies as a function of applied voltage, is probed by an incident mode-locked infrared probe pulse as a doubled blue pulse excites the detector. We measured the time response for four different finger-spacing detectors and the resulting traces for two of these detectors are shown in figure 1(b). We also estimate a capacitance of ~ 2 fF for minimum sized detectors. These rise-time measurements confirm the high speed operation of low capacitance CMOS detectors (~ 35 ps rise-time for the minimum finger-spacing case), which verifies the operation of such low capacitance detectors, and shows such devices should be suitable for very precise optical clock injection with Silicon CMOS.

[1] P. Kapur, K. C. Saraswat, "Optical interconnects for future high performance integrated circuits", in *Physica E: Low-dimensional Systems and Nanostructures*, Volume 16, Issues 3-4, March 2003, Pages 620-627.

[2] A. Bhatnagar, S. Latif, C. Debaes, D. A. B. Miller, "Pump-Probe Measurements of CMOS Detector Rise Time in the Blue", in *Journal of Lightwave Technology*, Vol. 22, No. 9, September 2004.