# Ring oscillators with optical and electrical readout based on hybrid GaAs MQW modulators bonded to 0.8μm silicon VLSI circuits

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*Indexing terms: Integrated circuits, Optical modulation, Flip-chip devices*

Loaded and unloaded ring-oscillator circuits with an electrical and surface-normal 850nm optical readout are fabricated using a hybrid 0.8μm silicon-CMOS/GaAs-AlGaAs MQW process. Measurements of the oscillation frequency of these circuits show total capacitance associated with the flip-chip-bonded optical MQW modulators as low as 52fF.

Technologies are now being developed for attaching GaAs/AlGaAs multiple quantum well (MQW) photodetectors and light modulators on to a prefabricated silicon integrated circuit using a hybrid flip-chip bonding technique followed by substrate removal of the GaAs chip to allow surface-normal operation of up to 2000 optical modulators at 850nm [1]. Fig. 1 presents the final structure of the hybrid circuit, and illustrates the three-dimensional nature of the integration.

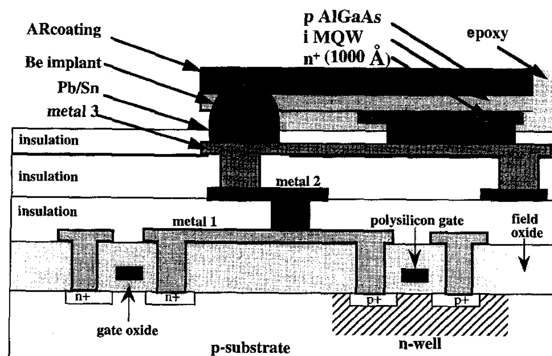


**Fig. 1** *Structure of hybrid GaAs MQW/silicon CMOS circuit*
Modulators may be bonded directly on top of active gates

Based on this process, we have recently implemented a 375Mbit/s receiver-transmitter circuit [2] and a 2Kbit first-in, first-out page-buffer circuit [3]. These initial results suggest that the hybrid CMOS-SEED (self electro-optic-effect device) technology could eventually provide a terabit-per-second of optical input/output to a conventional silicon VLSI integrated circuit. An important issue that affects the operation frequency and power dissipation of the resulting hybrid CMOS-SEED circuits is the capacitance of the MQW modulators, the bonding pads, and any interconnect line connecting the VLSI circuits to the MQW diodes. Here, we address this issue quantitatively by examining the effect of loading ring oscillator circuits with these capacitive elements.

Several ring-oscillator circuits were designed and fabricated in 0.8μm CMOS through the MOSIS foundry service. A unity-fanout, seven-stage ring-oscillator circuit with optical readout was tested to verify optical operation of the circuit and to measure the gate delays. This optical-readout technique has previously been used to test ring oscillators fabricated in a monolithic optoelectronic technology [4]. At one point in the ring, an inverter drove both the next inverter in the loop as well as the gates of an additional inverter circuit consisting of a 3× NMOS device and a 9× PMOS device. This inverter constituted the input stage of a three-stage transmitter buffer circuit. The transmitter encoded the output of the ring-oscillator on to a pair of optical output diodes using differential encoding. The output of the differential reflection-mode MQW modulators was optically monitored; one of the beams was sent to a detector and spectrum analyser. Fig. 2 shows the output of the modulator oscillating at 638.2MHz corresponding to a gate delay of ~112ps. Measurement of an identical, unloaded, seven-stage ring-oscillator circuit switching at 693.6MHz indicated a best-case, unity fan-in, unity fan-out, gate delay of 103ps. This switching frequency was measured by capacitively coupling the feedback element from the last to the first stage to a metal line connected to a probe pad. SPICE simulations have verified that the additional 9ps gate-delay of the optical-readout ring-oscillator circuit is caused by the added capacitive loading due to the transmitter circuit.

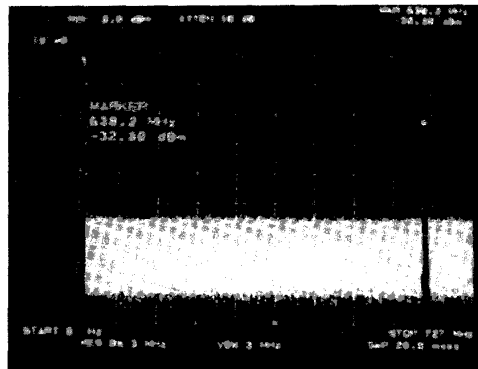

**Fig. 2** *Output of 7-stage ring oscillator circuit loaded with modulator driver buffer and modulator, operating at 638.2MHz*
Corresponding gate delay = 112ps. Output of modulator was monitored optically with a readout beam and focused on to a detector; output of detector was fed into a spectrum analyser

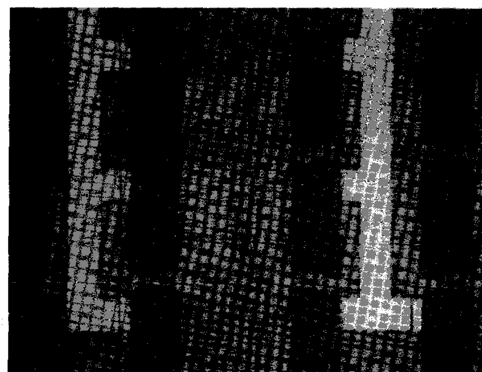

**Fig. 3** *Microphotograph of 0.8μm ring oscillator circuit loaded with 26μm × 26μm pads and MQW modulators after bonding and substrate removal*
*n*-contact pads of modulators are tied to a 10V supply for reverse-biasing. *p*-contact signal pads of diodes are attached to ring-oscillator. Diodes are ~20μm × 45μm. Active area of MQW modulator is ~17μm × 18μm

The capacitance associated with the hybrid CMOS-MQW diodes results mainly from the metal pads used for flip-chip bonding, the MQW diode with solder bond, and the interconnect line from the pad to the receiver or transmitter circuit [5]. To determine the contribution from the pads, we measured switching frequencies of ring-oscillators with each inverter stage loaded with identical pads, and compared them to the unloaded circuits. Gate-delays of three ring-oscillator circuits with 26μm × 26μm pads, 19μm × 19μm pads and 15μm × 15μm pads were 131ps, 124ps and 121ps, respectively. These measurements correspond to pad capacitances of 22fF, 17fF and 14fF, respectively. The scaling of these pad sizes represents improvements in the MQW diode structures and the precision and yield achievable with the hybrid integration process. Next-generation CMOS-SEED circuits will use 10μm × 10μm flip-chip pads with an expected pad capacitance of ~6fF.

The capacitance of the flip-chip bonded MQW diode was determined by comparing oscillation frequencies of bonded and

unbonded ring oscillator circuits. A nine-stage, unity fan-in, unity fan-out ring oscillator, with each inverter in the ring attached to 26μm × 26μm pads, was measured before and after bonding. Titanium, nickel and gold metals were deposited on to these pads; the CMOS chip was then aligned and flip-chip bonded to a GaAs chip containing 17μm × 18μm GaAs/AlGaAs MQW diodes. Following this, the GaAs substrate was removed, leaving behind *p-i*(MQW)-*n* diodes attached to their respective contact pads. Fig. 3 shows a microphotograph of the loaded 0.8μm ring oscillator circuit with attached pads and modulators after bonding and substrate removal. Each modulator required one pad for the *n*-contact, and one for the *p*-contact; the centre-to-centre spacing between the two corresponding pads was 30μm. The active area of each MQW diode (above the *n*-contact pad) was 17μm × 18μm. During normal operation, the diode is reverse-biased, so that the *n*-contact pad is tied to a positive voltage (typically 10V). The widths of the PMOS and NMOS of each inverter in the ring-oscillator were 5.1μm and 2.2μm, respectively; all transistors were minimum length (0.8μm). A switching frequency of 143MHz (389ps gate-delay) was obtained for the 9-ring oscillator loaded with the pads and the additional wiring to the remote modulators. The speed of the circuit loaded with the MQW modulator and solder-bond was measured at 107MHz (521ps gate-delay). Simulations indicate that the additional delay corresponds to a capacitive load of ~38fF. This is in agreement with previous analytical estimates of the SEED capacitance that indicate a capacitance of ~0.11fF/μm² [5]. In addition, the speed of the circuit after bonding but before substrate removal was measured at 104MHz (534ps); this corresponds to a difference of ~4fF. This suggests that the substrate removal process may improve the performance of the MQW devices by eliminating the parasitic diode-to-substrate capacitance. Thus the total capacitance of each MQW device, including the solder-bump bond and a 15μm × 15μm pad, but not including the interconnect line, was measured to be ~52fF. A 100μm interconnect line in the top-level metal layer to the remote modulator would increase this capacitance by ~10fF, depending on the specific circuit layout.

In conclusion, we have fabricated and tested 0.8μm ring-oscillator circuits with electrical and optical readout based on the hybrid silicon-CMOS/GaAs-AlGaAs MQW process to characterise the capacitance associated with a flip-chip bonded MQW diode. For the optically monitored 7-stage ring-oscillator circuit, a gate delay of 112ps was observed. Best-case gate delays of 103ps for an unloaded, unity-fanout ring oscillator were obtained. As a measurement technique, optical readout represents a useful means of measuring ring oscillator delays, at the expense of some added capacitive loading that should be taken into account. In order to determine the effect of scaling the size of the flip-chip bond pads, we have implemented ring oscillators loaded with pad sizes of 25μm × 27μm, 19μm × 19μm and 15μm × 15μm, respectively. Gate delays of ~121ps, 124ps and 131ps were measured for these circuits, corresponding to pad capacitances of 22fF, 17fF and 14fF, respectively. Next, we fabricated ring oscillators loaded with flip-chip pads and MQW modulators at each stage to investigate the capacitance of the MQW modulator and solder-bond. SPICE simulations based on measured gate delays indicate that the total capacitance of the flip-chip bonded MQW diode (with a 15μm × 15μm pad) is ~52fF. Such capacitances are low for any optoelectronic device in a circuit. Low capacitance is critical for improving receiver performance and reducing transntitter power. This capacitance is also very low compared to typical pad capacitances of picofarads or more, incurred with electrical off-chip connections. This makes the CMOS-SEED technology a promising candidate for VLSI systems that require high-performance off-chip I/O.

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## Sensitivity-based CMOS VLSI circuit performance optimisation

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*Indexing terms: CMOS integrated circuits, Optimisation, Sensitivity analysis*

Sensitivity models are presented for propagation delay and average power dissipation which provide low-cost and accurate differential performance information not previously available. A sensitivity-based optimisation technique is compared with a formal mathematical optimisation technique and the results demonstrate that accurate VLSI circuit performance optimisation is now feasible.

*Introduction:* VLSI circuit performance optimisation is restricted by the accuracy and cost of performance estimation. In addition, the formulation of a design specific single-objective function, comprising the conflicting characteristics propagation delay and average power dissipation, required by most mathematically based optimisation techniques, ensures relatively poor optimiser convergence due to a lack of differential information [1 – 3]. During the past decade attempts at estimating CMOS performance characteristics have resulted in process dependent models requiring the application of SPICE analysis and data fitting techniques [4]. More recently, the development of CMOS process independent propagation delay and average power dissipation models [5, 6], has facilitated the development of CMOS performance sensitivity models. Normalised macro sensitivity values directly relate the sensitivity of a performance characteristic to a parameter change, to all other macro sensitivity values within a circuit, providing low cost and accurate differential performance information not previously available.

*Sensitivity models:* The process dependent nature of earlier propagation delay models prohibited any attempt to perform sensitivity analysis [4]. However, the process independence of the recently reported CMOS propagation delay and average power dissipation models has enabled their symbolic differentiation with respect to the width of each macro resulting in the delay and power sensitivity models shown in eqns. 1 and 2, respectively.