Monolithic Integration of GaAs/AlGaAs Multiple Quantum Well Modulators and Silicon Metal-Oxide-Semiconductor Transistors

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Abstract- We demonstrate coexisting operation of a GaAs/AlGaAs multiple quantum well modulator and a submicron gate length metal-oxide-semiconductor transistor fabricated on the same chip, for applications in optical interconnects.

It is now generally recognized that one likely scenario in which photonics is used in a switching environment is where it is integrated with electronics.[1] This concept takes advantage of the greater capacity of electronics for complexity, functionality, and memory, and the greater capacity of photonics for communications. The most concrete realization of this concept is where photonics functions in the role of optical interconnects between electronic integrated circuit chips (ICs). This entails the monolithic integration of some photonic elements (both receiver and transmitter) on the chip. Also, since an attractive feature of optical I/O is that it can occur normal to the surface of the chip, allowing two-dimensional arrays of interconnects to be formed, surface-normal photonic elements should be used.

Silicon electronics seems to be the most effective technology where complex systems such as microprocessors or memory is concerned. Since the benefit of increased communication capacity to the chip is most attractive when the chip contains a great number of computing elements, it appears that the strongest impact of photonics will be as optical input/output for silicon integrated circuits.

Furthermore, intimate integration of the photonic elements must be achieved with the transistors (i.e., the photonic device must be placed within microns of the electronic device), or else the capacitance of the interconnecting metal lines will degrade the speed advantage that photonics offer. In addition, thousands of photonic devices should be integrated on the chip to take full advantage of the parallelism of optics. Since III-V based photonic elements offer the only high-speed (i.e., GHz), high efficiency operation, and these attributes are necessary for optics to displace electron interconnect technology, it appears that direct heteroepitaxial growth of III-V photonic elements on Si ICs offers the best possibility for the use of photonics in switching systems.

Finally, simultaneous operation of large arrays (e.g., thousands) of surface-emitting lasers has not been demonstrated, and their operation would be thermally problematic, whereas such arrays of surface-normal modulators have been demonstrated.[2] No surface-normal laser heteroepitaxially grown on silicon has been demonstrated at all, whereas reliable surface-normal modulators have been produced on silicon.[3,4] All this information can be summed up with the statement that one logical infiltration of photonics into switching will be in the form of surface-normal modulators grown on silicon ICs functioning as optical interconnects. This function is achieved by

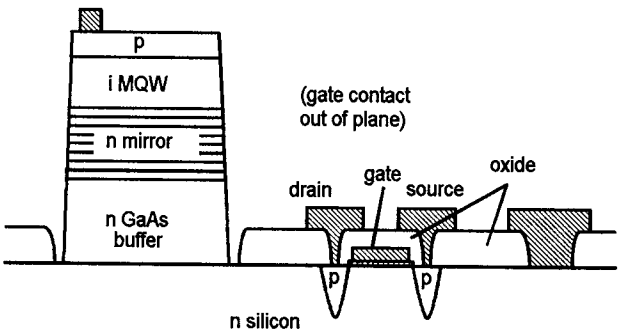

Fig. 1: Schematic of our GaAs/AlGaAs modulator integrated with the PMOS silicon transistor.

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modulating the reflectance of beams from an off-chip laser which has been split into an array of spots. This offers the further system advantage over lasers of a global clock (oscillating the off-board laser). Also, quantum well modulators have the advantage of being highly efficient detectors, eliminating the need for integrating two types of photonic devices or using inferior silicon detectors.

Having demonstrated the physical ability of placing reliable modulators on silicon substrates, it remains to show that they may be grown on silicon ICs while retaining the function of the silicon transistors. (It is generally thought that the transistors should be made first since higher processing temperatures are incurred making them, and also since Ga is a notorious impurity for silicon electronics.) In this paper we take the first step toward demonstrating this ability. We have grown and tested a multiple quantum well (MQW) modulator on a silicon IC which was obtained from a standard 0.9 μm linewidth fabrication line. The modulator functioned, although with reduced performance due to spectral misalignment of the integral mirror with the exciton of the MQW. We then metalized and tested a 20 μm gate length transistor on the IC (the reason why the shorter gate length transistors have not been tested will be discussed below) and it functioned near the specifications of the fabrication line.

The modulator growth was performed on a silicon IC obtained from an AT&T Microelectronics facility. It had individual test CMOS transistors fabricated on it using 0.9 μm linewidth rules.[5] The transistors had gate lengths ranging from 0.75 to 20 μm, however, all had drain and source openings that were 0.9 X 20 μm. The transistors we used were p-channel devices fabricated in n-"tubs" implanted into the p-type silicon wafer. Their gate oxides were 150 Å-thick. The wafer was oriented 3° off-axis from the (100) direction. This is because it has widely been found that off-axis Si substrates are necessary for quality GaAs growth. The wafer was removed from the silicon process line before the final metalization was performed. A SiN_x diffusion barrier was deposited on the chip to protect its field oxide from Ga absorption during growth.[6] Then a window was etched down to the silicon surface for modulator growth (Fig. 1). After dipping in dilute hydrofluoric (HF) acid to remove any non-native oxide from the growth window, the chip was loaded into a Gas-Source Molecular Beam Epitaxy (GS-MBE) reactor. Under vacuum it was heated to 850 °C to desorb the native oxide. The growth was then performed using a two-step process.

First, a 0.5 μm-thick low-temperature (350 °C) n-type GaAs buffer layer was deposited to make the transition from three-dimensional to two-dimensional epitaxy. Then a 1.5 μm-thick standard-temperature (600 °C) n-type GaAs buffer layer was deposited to reduce defect density. A 14.5 period 722/603 Å AlAs/$Al_{0.07}Ga_{0.93}As$ n-mirror was grown, followed by the i-MQW, which consisted of 60 periods of 95/35 Å GaAs/$Al_{0.3}Ga_{0.7}As$. Finally a 0.5 μm thick p-type $Al_{0.3}Ga_{0.7}As$ layer was grown. At the surface a p^{++} delta-doped GaAs layer was grown. Then the sample was cooled to 100 °C and a layer of Al was deposited for the top contact.[7] This Al tunneling ohmic contact allows for compatibility with the Al-based metalization of silicon electronics.

After removal from the reactor, the top contact of the modulator was defined by photolithography and etching using a 100:1 H_2O:HF etch. The growth resulted in deposition of non-crystalline material on the area outside the growth window. This was removed by defining a photoresist mask on the modulator and using a wet etch. The final size of the modulator was 60 X 80 μm. As shown in Fig. 1, the bottom contact to the modulator was made by defining a contact to the silicon on the top surface of the chip. We have shown that modulators with contacts independent from the substrate (i.e., isolated) may be grown by using undoped GaAs buffer layers, in the case that several independent modulators must be placed in the same silicon tub.[8]

The gate metal is a doped poly-Si runner that extends out of the plane of Fig.1 to where it is exposed for contact. The gate and runner were fabricated in the silicon processing facility. After defining openings in the silicon nitride diffusion barrier to the gate, source and drain contacts, we deposited Al electrodes as shown. Finally the contacts were annealed at 350 °C. Note that metalizing to the drain and source contacts requires patterning of photolithographic features nearly the same size as the transistor gate. Because of the height of the modulator above the silicon surface (about 6 μm), there exists a large gap between the photomask and the photoresist on the silicon transistor surface during contact lithography. This leads to diffraction of the light during exposure and thus difficulty in defining micron-size features. Therefore, we first produced chips with only the 20 μm gate length transistor metalized.

The modulator characteristics are shown in Fig. 2. Unfortunately, the mirror was spectrally misaligned relative to the exciton. As can be seen in the figure, the mirror edge is at 863 nm, whereas the exciton is about at 850 nm. It is not clear whether this was a simple error or if recalibration of growth rates must be performed for selective area growth on silicon. Even though the mirror was misaligned, with 15 volts bias the exciton of the MQW shifts far enough to modulate

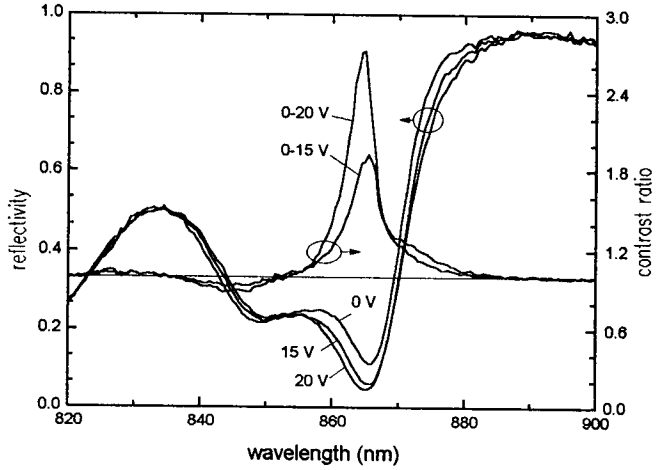

Fig. 2: Reflectivity of our modulator at different reverse biases. Unfortunately the mirror was misaligned with the exciton, reducing performance.

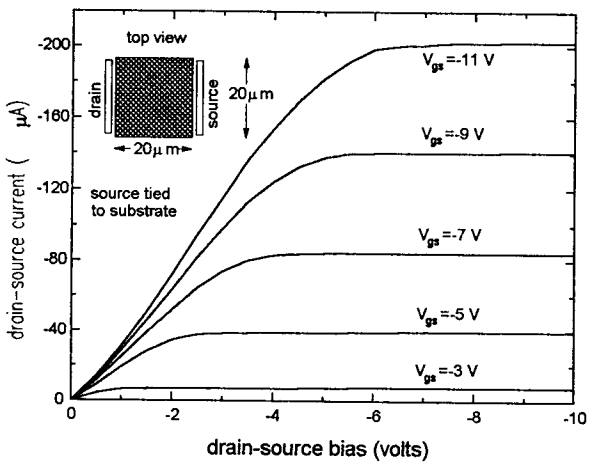

Fig. 3: Common-source characteristics of our 20 micron gate length PMOS silicon transistor.

the reflectivity at the mirror edge. With 20 volts bias, we in fact achieve nearly 3 to 1 contrast ratio.

The transistor characteristics are shown in Fig. 3. Reasonable field-effect transistor characteristics are obtained, albeit with some contact resistance which can be observed in the negative bowing of the turn-on of the Vgs=-11 V curve. This contact resistance could be due to inadequate coverage of metal in the contact holes or due to damage incurred when the silicon nitride was removed from the contact holes. Fig. 4 shows the transconductance of the transistor ($dI_d/dV_g|_{Vds=-8V}$). The threshold voltage is -1.56 volts. The specified value is -1.1 volts.[5]

As mentioned, there is difficulty in metalizing the micron gate length transistor because of diffraction of light during contact lithography caused by the large topograpy of the modulator. There are various options that may solve this problem: 1) The modulator could be recessed by etching and growing in a hole.[9] However, the modulator can only be recessed as deep as the n-tub implantation, which is about 1.5 μm. Therefore without modification of the silicon processing technology this is only a partial solution. 2) The mirror may be replaced with an implanted silicide reflector, reducing the total modulator thickness.[10] Again, this is only a partial solution and also requires that the silicide be implanted before the silicon processing.[10] 3) A tri-level resist technology may be used, where thick resist is spun on the wafer, resulting in a planar surface. A metal layer is deposited on this resist, is patterned, and dry-etching is then used to remove the resist around the pattern. This adds a great deal of complexity to the processing. 4) Projection lithography is used. Projection lithography is an expensive technology available in silicon processing lines, and would thus entail re-entering the chip into the silicon processing line after GaAs deposition and therefore introduce possibility of contamination into the line. All of these options are being explored.

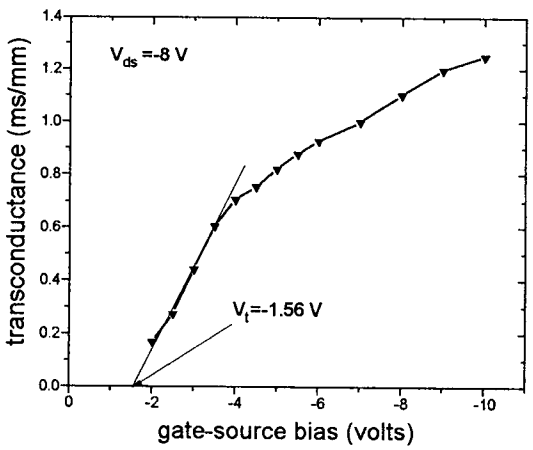

Fig. 4: Transconductance of our 20 micron gate length transistor as a function of Vgs. The threshold voltage is near the specified value of -1.1 V.

However, we present here a solution that is simpler in concept but more complicated in practice because it adds to the number of processing steps. After spinning resist onto the chip, separate exposures are used to define the source and the drain contacts using a mask with a single hole pattern. The hole is positioned further away from gate than the actual gate-drain spacing, so that even though diffraction occurs, a narrow strip of resist is left above the gate. By using separate exposures for the source and drain, the extra spacing neccessary to acheive this can be determined empirically. One could in principle design this into a mask with two holes in order to make a single exposure possible. However, since this is a lift-off process for defining the contacts (the metal is deposited after the photoresist and then "lifted-off" the areas where photoresist remains), which has been shown to have less resolution than the etch process (wherein the metal is deposited before the photoresist and etched from the regions where photoresist is removed), it is not clear that this is the final solution.

In any event, we were able to pattern the micron gate length transistor and show its characteristics in Fig. 5. Note the much higher currents obtained compared to the 20 micron gate length transistor. Fig. 6 shows the transconductance of the transistor. The threshold value of -2.4 V is again near the specified value.

In conclusion, we have demonstrated monolithic integration of a GaAs/AlGaAs surface-normal reflection multiple quantum well (MQW) modulator

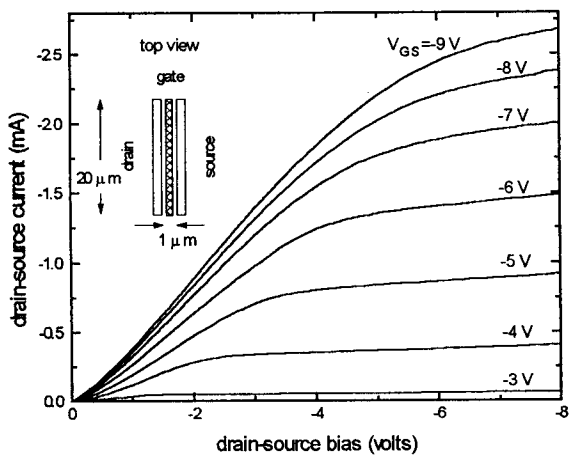

Fig. 5: Common-source characteristics of our micron gate length PMOS silicon transistor with integrated modulator.

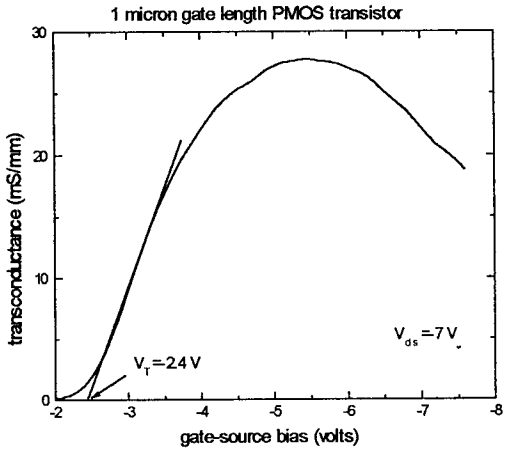

Fig. 6: Transconductance of our micron gate length transistor vs. Vgs.

and a micron gate length silicon metal-oxide-semiconductor transistor. We obtain nearly 3 to 1 contrast for the modulator, whose performance was degraded because of spectral misalignment of the mirror with the MQW exciton. The transistor's characteristics have not shifted greatly from its specified values. This shows that practical integration of modulators on Si IC's may be done, paving the way for optical interconnects in silicon based switching systems.

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