Logic Self-Electrooptic Effect Devices: Quantum-Well Optoelectronic Multiport Logic Gates, Multiplexers, Demultiplexers, and Shift Registers

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Abstract—**We demonstrate two-dimensional arrays of logic self-electrooptic effect devices (L-SEED's), consisting of electrically connected quantum-well p–i–n diode detectors and modulators. The topology of the electrical connections between the detectors is equivalent to the connections between transistors in CMOS circuits. Three different L-SEED arrays were built and tested. Each element in one array can implement any of the four basic Boolean logic functions (i.e., NOR, NAND, AND, OR). Each element in the second L-SEED array can implement the function $E = AB + CD$. The third L-SEED array consists of 32 × 16 arrays of symmetric SEED's (S-SEED's) connected with optoelectronic transmission gates. Photonic switching nodes, multiplexers, demultiplexers, and shift registers have been demonstrated using this array.**

Introduction

ARCHITECTURES for optical information processing have been the subject of intense research for several years. One class of architectures uses two-dimensional arrays of optical or optoelectonic logic gates with optical interconnections between the arrays normal to the surface. Quantum-well self-electrooptic effect devices (SEED's) [1] have emerged as a leading candidate for use in systems that implement these architectures. Arrays of symmetric SEED's (S-SEED's) [2] as large as 128 × 256 (32 K elements) [3] have been made and 64 × 32 arrays [4] are now commercially available. System demonstrations using these devices have begun to appear [5], [6]. These devices have many attributes that make them desirable from a systems point of view. The devices are differential in nature, and the logical states of the inputs and outputs are defined by the ratio of optical powers in a set of two beams. This allows operation over several decades in optical power and allows gain without critical biasing. Recently, we have made 64 × 32 arrays of S-SEED's that operate over a range of optical powers from less than 5 nW to greater than 500 μW per device. In operation, the state of the devices is set using a pair of low power signal beams and subsequently read using a pair of higher power clock beams. The devices have high gain because the optical powers of the clock beams can be greater (limited by the above range of powers) than the optical powers of the signal beams. This gain allows experimental optical processing systems to be demonstrated, even in the presence of considerable losses in the interconnection optics between device arrays. Because a set of clocked power beams is used to read the state of the device, logic level restoration, re-timing, and wavefront quality restoration are done at each stage for systems containing several device arrays. The S-SEED's have the characteristics of a set-reset latch and can perform any of the four basic Boolean logic functions by using a preset beam [2].

While optical processing systems can be built using NOR gates alone, systems using logic gates of more complex functionality may enable more optimal systems to be built, that is, systems that require less laser power per device array, fewer device arrays, fewer optical components, or offer more tolerance to signal variations or mechanical misalignments. We can design SEED's with arbitrary logical functionality using a separate group of quantum-well detectors configured similarly to the field effect transistors in CMOS and NMOS circuits to drive a S-SEED configured as an output modulator [7]. We call these SEED's, logic SEED's (L-SEED's).

In this paper, we will describe 16 × 16 arrays of L-SEED's with each element performing any of the four basic logic functions without using the preset beam that is required with a S-SEED logic gate and 4 × 4 arrays of L-SEED's with each device acting as a switching node or exclusive OR gate. We also extend the L-SEED concept to SEED's containing optoelectronic transmission gates,

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which are analogous to transmission gates in CMOS circuits. We describe a 32 × 16 array of S-SEED's with neighboring S-SEED's connected by these optoelectronic transmission gates. Using this array, we demonstrate a 2 × 1 switching node, a multiplexer and demultiplexer, an 8 × 16 array of 2 × 1 switching nodes operating concurrently, and an 8 bit shift register.

L-SEED Logic Gate

In this section, we will describe L-SEED's in general and discuss the array of L-SEED logic gates. The basic concept of a L-SEED is illustrated in Fig. 1. The L-SEED consists of a group of input diodes with incident input signal and a pair of output diodes (i.e., a S-SEED) that modulates a pair of equal power clock beams to provide the output. The input diodes need not have quantum wells [7], although the devices can be made using the same batch fabrication techniques as the S-SEED's [9] when all diodes have quantum wells. In this paper we will only consider the differential L-SEED's in which a pair of beams represents the logic state of the inputs, although devices whose logic state is represented by the power levels of a single beam could also be made [7].

For differential L-SEED's, the topology of the electrical connections between input diodes is identical to that of CMOS circuits [8]. To obtain the required L-SEED layout, the n-channel devices in a CMOS circuit are replaced by diodes with incident uncomplemented signal inputs and the p-channel devices in the CMOS circuit are replaced by diodes that have complemented inputs. Several design examples are found in [7].

Differential L-SEED's have two groups of p–i–n diodes that accept the incident input signals. These are shown in Fig. 2 as group 1, with uncomplemented input signals, and $\overline{\text{group 1}}$, with complemented input signals. Group 1 and $\overline{\text{group 1}}$ are connected electrically in series. The diodes in $\overline{\text{group 1}}$ are electrically interconnected in a manner known as the conduction complement [8] of the connections of the diodes in group 1. For example, if group 1 consists of serially connected diodes then $\overline{\text{group 1}}$ consists of parallel-connected diodes. The voltage at the interconnecting node between group 1 and $\overline{\text{group 1}}$ is connected to the center node of an output S-SEED, and thus determines the output state of the device. Each logical input uses two complementary beams to represent the logic state. If the power of the uncomplemented beam is greater than the complemented beam this input will be defined as logic "one"; a logic "zero" is the reverse case. For noninverting functions (i.e., AND's and OR's), output C is the uncomplemented output, and output $\overline{C}$ is the complemented output. For inverting functions (i.e., NAND's and NOR's), the outputs are reversed. That is, the output labeled C becomes the complemented output, the output labeled $\overline{C}$ becomes the uncomplemented output. In either case, we define the output state to be a logic "one" when the power of the uncomplemented output beam is greater than that of the complemented output beam.

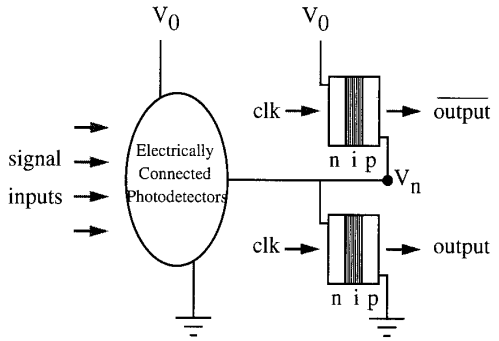

Fig. 1. Logic self-electrooptic effect device (L-SEED). In the devices that we describe here, the electrically connected photodetectors are also quantum-well p-i-n diodes.

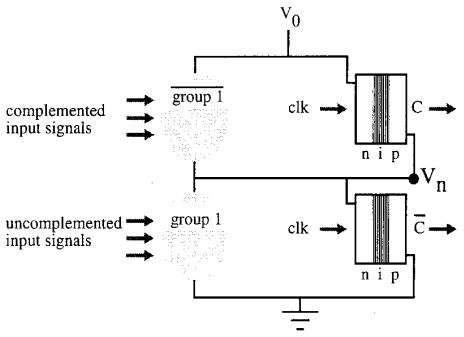

Fig. 2. Differential L-SEED showing the two groups of input diodes. Each input is represented by a pair of complementary beams. Group 1 has the uncomplemented inputs and $\overline{\text{group 1}}$ has the complemented inputs.

In operation, first the signal beams are applied to the respective diodes. The voltage that will be present on the node between the two groups of "signal" diodes, V_n in Fig. 2, will be a function of the currents generated by these diodes. V_n will be essentially zero if the photocurrent generated by group 1 is initially greater than that generated by $\overline{\text{group 1}}$. This is illustrated in Fig. 3(a) where the solid line represents the photocurrent generated by the diodes in group 1 and the dashed line represents the photocurrent generated by the diodes in $\overline{\text{group 1}}$. Conversely, V_n will be essentially equal to the supply voltage if the photocurrent generated by group 1 is initially less than that generated by $\overline{\text{group 1}}$ as illustrated in Fig. 3(b).

The node between the two groups of input diodes is electrically connected to the node between the two diodes of the output S-SEED. Therefore, once the voltage at this point has been determined (i.e., after the switching time of the circuit), we can remove the signal beams and apply the clock beams of higher power achieving time-sequential gain. The L-SEED's must be operated near the wavelength of the exciton peak at zero volts, so that the device is bistable when the clock beams are applied. A typical plot of the output reflectivity versus voltage at this wavelength is shown in Fig. 3(c). For the case described for Fig. 3(a) where V_n is essentially zero, output $\overline{C}$ (in Fig. 2) will be "low" and output C will be "high". For the

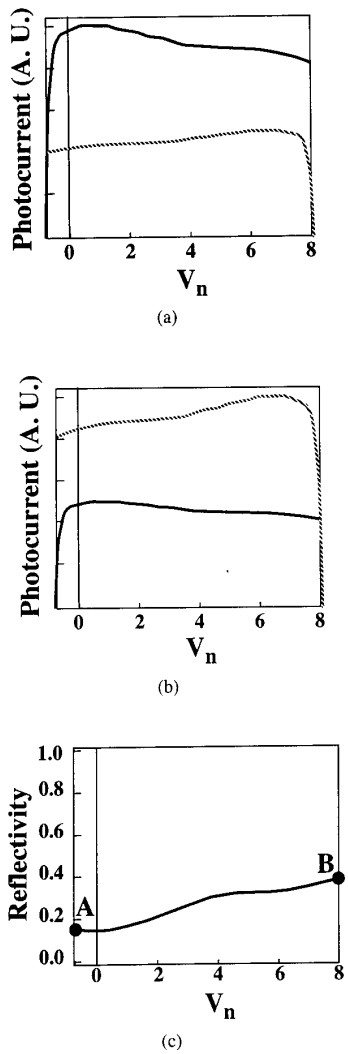

Fig. 3. Photocurrent versus voltage V_n for group 1 (solid lines) and group $\overline{1}$ (dashed lines). (a) Current from group 1 is greater than that of group $\overline{1}$. (b) Current from group 1 is less than that of group $\overline{1}$. (c) Reflectivity versus voltage for the quantum well diodes. Point A corresponds to case (a) and B corresponds to (b).

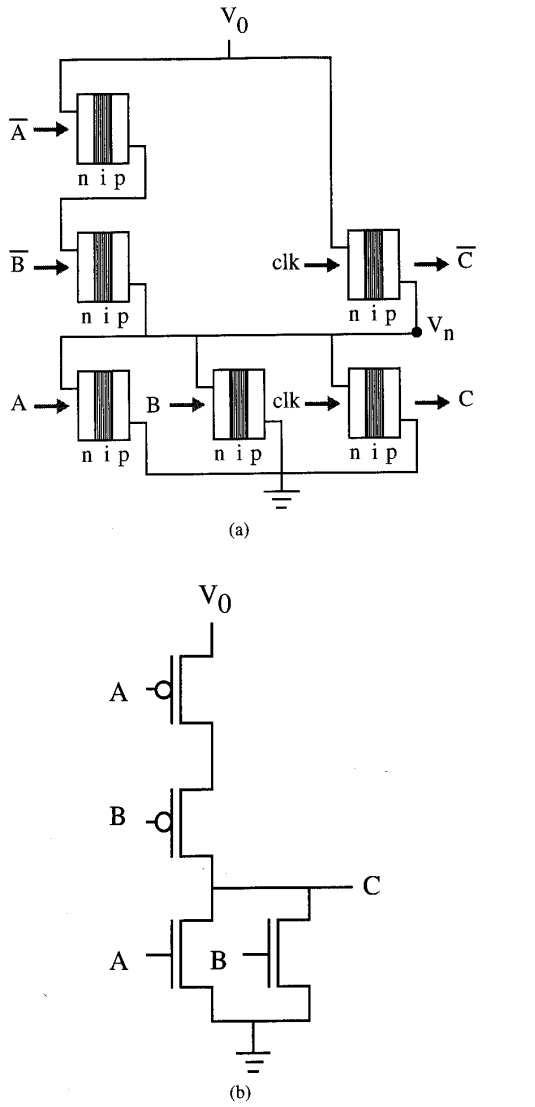

Fig. 4. (a) Differential L-SEED NOR gate schematic diagram. The two inputs and the outputs are logic "ones" when $A > \overline{A}$, $B > \overline{B}$, and $C > \overline{C}$. Devices are shown schematically as transmission mode devices, but the actual devices were reflection mode devices. (b) CMOS NOR gate.

case described for Fig. 3(b) where V_n is essentially equal to the supply voltage, output $\overline{C}$ will be "high" and output C will be "low".

As an example, consider the differential L-SEED logic gate configured as a NOR gate and shown in Fig. 4(a). The CMOS NOR gate is shown in Fig. 4(b). Each logic gate consists of six quantum-well p-i-n diodes, four diodes are input diodes and two diodes are output diodes. Although we will describe the operation as a NOR gate, the other three logic functions (NAND, AND, OR) can be implemented by interchanging the inputs and/or outputs of the logic gate. In making systems with this device, signals are routed in pairs with their logic state determined by the ratio of the optical powers in the two beams. For NOR operation, we define a logic "one" when $A > \overline{A}$, $B > \overline{B}$, and $C > \overline{C}$. The uncomplemented signals, A and B, are incident on the parallel connected diodes (group 1 in Fig. 2), and the complemented signals, $\overline{A}$ and $\overline{B}$, are incident on serially connected diodes (group $\overline{1}$ in Fig. 2). If input A, input B, or both inputs are "high", either or both inputs $\overline{A}$ and $\overline{B}$ must be low. Initially more current will flow through the parallel connected diodes than the serially connected ones, so the center node voltage V_n will tend to switch toward 0 V. Thus, when the clock beams are applied output C will be low. However, if both inputs A and B are low, the serially connected diodes will generate more initial current than the parallel connected diodes and the node voltages V_n will switch toward V_0 V. Therefore, output C will be high when the clock beams

are applied. This operation has the characteristics of a NOR gate. Any differential NOR gate can perform AND, OR, and NAND functions by redefining the logic state of the inputs and/or outputs. For example, if we define a logic "one" when $A < \overline{A}$, $B < \overline{B}$, and $C < \overline{C}$, then the logic gate is a NAND gate. Unlike the S-SEED logic gate which can change its function, for example from a NAND to a NOR gate, by selectively using one of two preset beams, the L-SEED logic gate cannot be *optically reconfigured* to change its function, once the input and output logic states are defined.

A 16 × 16 array of L-SEED logic gates was made using the same batch fabrication procedures as the arrays of S-SEED's [3], [4], [9]. The material was grown by molecular beam epitaxy. A photograph of part of the array and a diagram of the layer structure are shown in Fig. 5(a) and (b). The devices are reflection mode devices [10] with 71.5 periods of 100 Å GaAs quantum wells and 35 Å $Ga_{0.7}Al_{0.3}As$ barriers. Each optical input and output window is 5 × 5 μm. The inputs and outputs (e.g., A and $\overline{A}$) are on 20 μm centers, and the different inputs (e.g., A and B) are on the 10 μm centers. Including the power leads, the unit cell size is 35 μm × 40 μm for a total array size of 560 μm × 640 μm. The unit cell size for S-SEEDs with 5 × 10 μm windows is 20 × 40 μm [3], [4]. The rectangular windows of the S-SEED allow for two signal beams and a clock beam within the same window but in the L-SEED separate windows are provided for all beams. Bistability data on S-SEED's from the same wafer showed a contrast ratio of 4:1 at 6 V increasing to 7:1 at 15 V at input powers of ~10 μW.

The L-SEED's were tested as logic gates by generating the input data using two differential quantum-well modulators, each of which is an S-SEED with an electrical connection to the center node [2]. These modulators were from a different wafer than the L-SEED's. The contrast ratios of the outputs from the modulators were ~2:1, which was lower than expected, perhaps due to saturation of the absorption of the quantum-well material as these modulators had thicker (65 Å) barriers [11]. For the gate to function correctly when switching from a logic "zero" to a logic "one" output state (i.e., V_n changing from ~0 V to ~V_0 V), the initial photocurrent flowing in the serially connected diodes with incident "high" signals must be greater than the initial photocurrent flowing in the parallel connected diodes with incident "low" signals. This implies that the input contrast ratio divided by two must be greater than the input contrast ratio at the edge of the bistable loop. By attenuating the inputs to the parallel connected diodes by 50%, optimum operation is achieved with low contrast inputs [7]. A diagram of the experiment is shown in Fig. 6. The data inputs from the differential modulators were reflected from an array of patterned mirrors (APM's) onto the optical windows of the device. The clock inputs and outputs passed through the transparent substrate between the mirrors. The mirror array had alternating rows of chromium and gold mirrors. The inputs incident on the parallel connected diodes were reflected

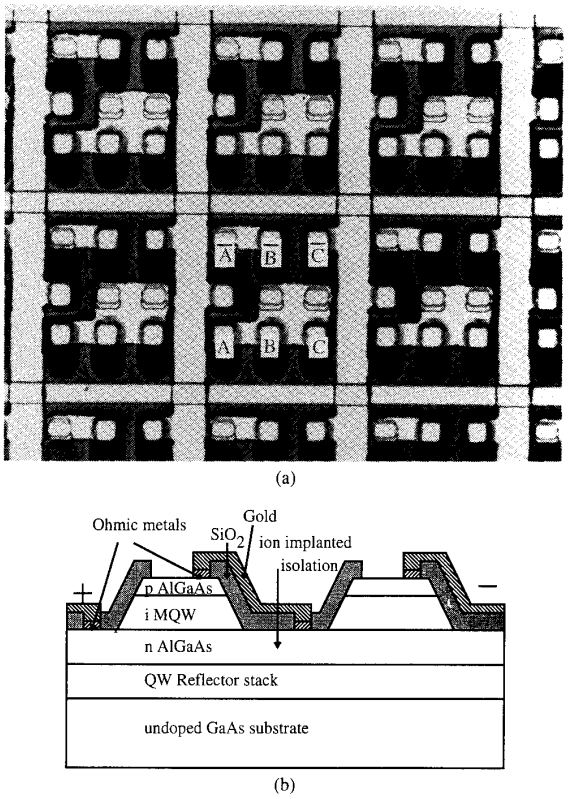

Fig. 5. (a) Photograph of a section of a 16 × 16 array of L-SEED logic gates. For NOR operation, input A, input B, and output C are located at the lower left, middle, and right of the unit cell, respectively, and their complements located above them. (b) Layer structure for the array: epitaxial layer dopings, compositions, and thicknesses (from bottom to top): reflector stack: 15 periods of alternating undoped AlAs 723 Å and $Al_{.11}Ga_{.89}As$ 599 Å with top $Al_{.11}Ga_{.89}As$ layer of 1198 Å; anode $n = 5 \times 10^{18}/cm^3$ $Al_{.11}Ga_{.89}As$ 5000 Å; buffer: undoped $Al_{.11}Ga_{.89}As$ 500 Å; MQWS: undoped 71.5 periods (71 wells 72 barriers) $Al_{.30}Ga_{.70}As$ 35 Å and GaAs 100 Å; buffer: undoped $Al_{.11}Ga_{.89}As$ 200 Å; cathode: $p = 5 \times 10^{18}/cm^3$ $Al_{.11}Ga_{.89}As$ 3000 Å; total thickness ~3.93 μm.

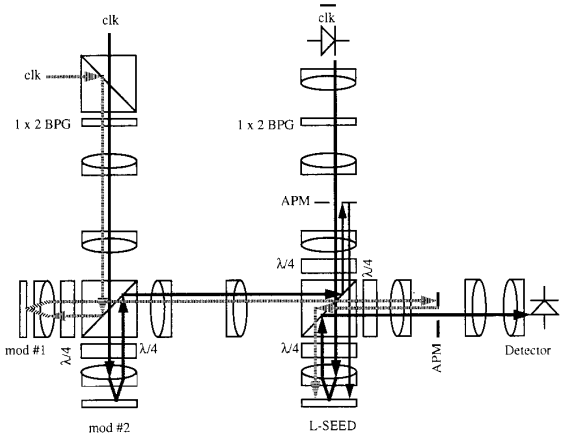

Fig. 6. Experimental setup for NOR gate demonstration. Symbols are defined as follows: BPG (binary phase gratings), APM (asymmetric patterned mirrors), λ/4 (quarter wave plate), mod #1, mod #2 (S-SEED differential modulators), *clk* and $\overline{clk}$ (optical inputs from lasers). All beam spitters are polarizing. Arrows show the paths of the optical beams and are not ray traces.

from the chromium mirrors, and the inputs incident on the serially connected diodes were reflected from gold mirrors. Since the reflectivity of the chromium mirrors was 56% of that of the gold mirrors, almost ideal attenuation was provided. It has also been shown that using the selective attenuation for inputs to a S-SEED operating as a logic gate increases the allowed variations in optical signal levels [6], [12].

The oscilloscope photograph in Fig. 7 showing the A and B inputs and the C output demonstrated that the device has the correct NOR functionality. The input powers on the device were ~ 2 and ~ 4 μW for the "low" and "high" states of the attenuated inputs A and B and ~ 4 and ~ 8 μW for the "low" and "high" states of the unattenuated inputs $\bar{A}$ and $\bar{B}$. The switching time for this and all subsequent experiments will be defined as the minimum time that the input signals could be applied for functionally correct and stable operation of the gate. This was measured by increasing the frequency (clock rate) of the word generator that controlled the modulation of the lasers until the output became unstable ("chattering") or was no longer functionally correct. For the NOR gate described here, this switching time was ~ 1 μs. The risetimes and falltimes of the oscilloscope traces in Fig. 7 (and also for the experimental results shown in Fig. 11, 15, 18, 20, and 22) are indicative of the modulation of the lasers by the word generator or in some cases the risetimes and falltimes of the detectors and are not related to the switching times or energies of the devices. We can define the differential energy as the difference in power level of the two inputs that make up a pair, for example A-$\bar{A}$, multiplied by the switching time. This is the amount of energy that would need to be supplied by a single beam incident on one of the parallel connected diodes to switch the device from a logic "one" to logic "zero" output state. Two beams of this energy would be required incident on the serially connected diodes to switch the device from a logic "zero" to logic "one" output state. Using the unattenuated powers, these energies correspond to (8–4 μW) $\times$ 1 μs or 4 pJ per data input for the device at 13 V bias. This energy is slightly more than a factor of two higher than that of a comparable S-SEED [3]. One reason for this is that the capacitance is estimated to be 1.5 times larger in these devices because there are six diodes as opposed to the equivalent area of four diodes in the S-SEED. A second reason is that when the inputs are attenuated, the equivalent difference in power is only 2 μW, thus giving an additional factor of two increase in the required energy.

The main advantage of the L-SEED logic gate over the S-SEED logic gate is that a preset beam is not required for logic functions. If preset beams are used in the L-SEED gate, there will be greater tolerance to signal beam nonuniformities compared to the S-SEED logic gate, although the L-SEED gate is not optically programmable even with preset beams. However, if we compare the tolerance to nonuniformity of the two gates when the S-SEED has a preset beam and when the L-SEED does not, or if the S-SEED has selective attenuators and the L-SEED does not, which device is more tolerant to nonuniformities will depend on the particular characteristics (i.e., contrast ratio and bistable loop width) of the devices.

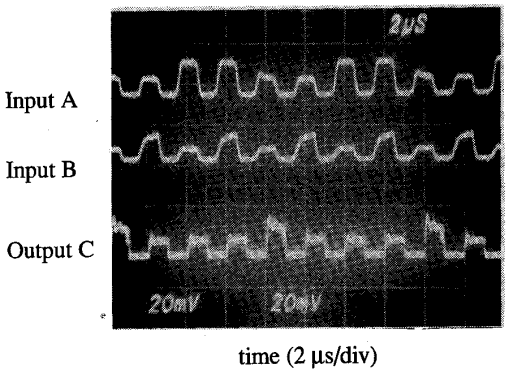

Fig. 7. Experimental results for a NOR gate demonstration, showing the uncomplemented inputs and output.

L-SEED $E = AB + CD$ GATE

Extending the simple L-SEED logic gates described in the previous section to more complex functions is illustrated in Fig. 8 [7]. In Fig. 8, groups of diodes labelled group 1 and group 1 implement funtion 1 and group 2 and group 2 implement function 2. Functions 1 and 2 may be simple functions like AND or OR or may be more complex functions. For the uncomplemented signals, the OR [Fig. 8(a)] and AND [Fig 8(b)] of two functions is achieved by electrically connecting their respective groups of p–i–n diodes with uncomplemented input signals in parallel and series, respectively. However, the groups of diodes with incident complemented signals are connected in series and parallel for OR and AND functions respectively. As before, the diodes with the uncomplemented inputs are connected in series with the diodes with the complemented inputs. The center node between these two groups of diodes is connected to the center node of the output S-SEED, and the voltage on this node determines the relative outputs of the S-SEED.

As an example, let us consider a function given by $E = AB + CD$. This function implements the exclusive OR of X and Y if $A = X$, $B = \bar{Y}$, $C = \bar{X}$, and $D = Y$. This same function implements a switching node with two data inputs and one data output (a 2 $\times$ 1 node) if A and C are the two data input channels and B and D are the two control channels. If control input B is a logic "1" and control input D is a logic "0", then output E is equal to data input A. Likewise, if control input B is a logic "0" and control input D is a logic "1" then output E is equal to data input C.

The differential logic gate shown in Fig. 9 implements this function. Group 1 consists of two diodes with incident input beams A and B connected electrically in series. Group 2 consists of two diodes with incident input beams $\bar{A}$ and $\bar{B}$ connected electrically in parallel. As we have

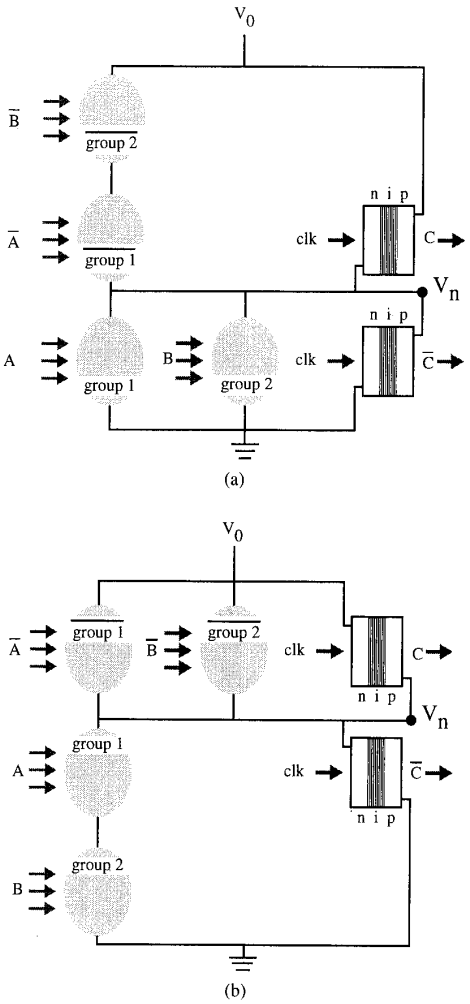

Fig. 8. Extension of L-SEED's to combinations of functions . (a) C = function 1 OR function 2 (A or B) (b) C = function 1 AND function 2 (A and B).

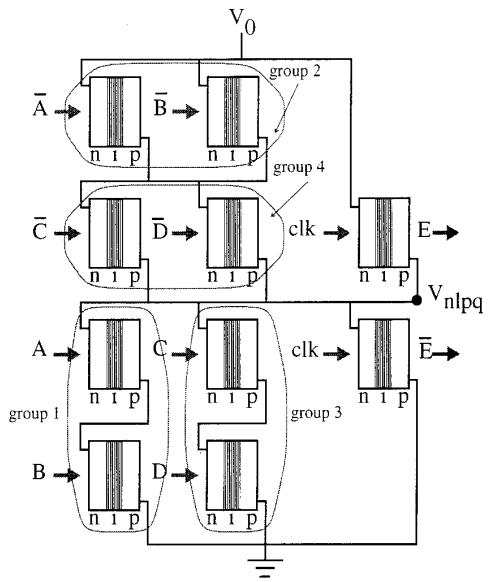

Fig. 9. Schematic diagram of a L-SEED gate implementing $E = AB + CD$. Devices are shown schematically as transmission mode devices, but the actual devices were reflection mode devices.

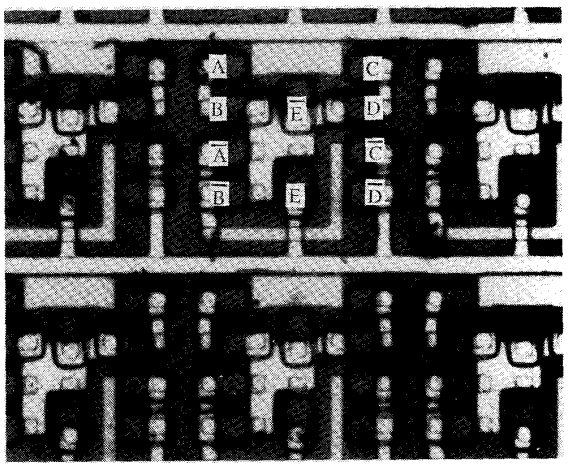

Fig. 10. Photograph of a section of the 4 × 4 L-SEED $E = AB + CD$ gate array. Diodes with metalization horizontal to the windows are the input diodes and diodes with the metalization vertical to the windows are the output diodes. A gate consists of eight input and two output diodes.

seen above, groups 1 and 2 implement an AND function of A and B. Similarly, group 3 consists of two diodes with incident input beams C and D connected electrically in series, and group 4 consists of two diodes with incident input beams $\overline{C}$ and $\overline{D}$ connected electrically in parallel. Groups 3 and 4 implement the AND function of C and D. To implement the OR of AB and CD, connect groups 1 and 3 in parallel and groups 2 and 4 in series.

A photograph of an array of L-SEED's that implements this function is shown in Fig. 10. The functionality of this circuit has been previously demonstrated by electrically connecting S-SEED's on different chips [7]. The integrated 4 × 4 arrays have 5 μm × 5 μm optical windows, with each pair of input and output windows on 20 μm centers. The unit cell size is (55 μm)^2 which was slightly larger than two S-SEED devices with 5 μm × 10 μm windows [3], [4], although three of these S-SEED's would be required to implement this function [13].

To demonstrate the operation of this gate, a 2 × 4 array of quantum-well modulators on the appropriate center to center spacings was used to generate independent input data for A, B, C, and D and their complements. We can define a logic "one" for each particular input when $A > \overline{A}$, $B > \overline{B}$, $C > \overline{C}$, $D > \overline{D}$, and $E > \overline{E}$. A clocked laser diode and two cascaded binary phase gratings provided the eight beams that were imaged onto the modulator array. The outputs of the modulator array were imaged directly onto the input windows of one element of the L-SEED array. A second laser diode provided the clock beams to read the state of the L-SEED. The results are shown in Fig. 11. The top four traces show four of the eight modulating voltages applied to the array of modu-

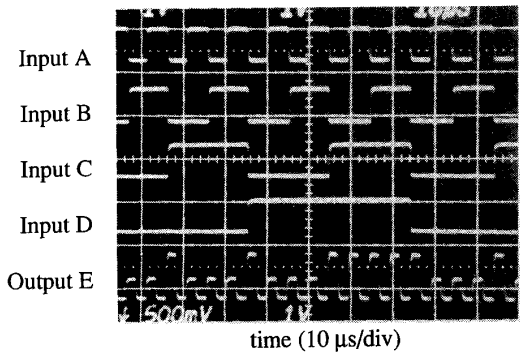

Fig. 11. Experimental demonstration of the function $E = AB + CD$. The top 4 traces are the modulating voltages applied to the four uncomplemented inputs and the bottom trace is the uncomplemented output.

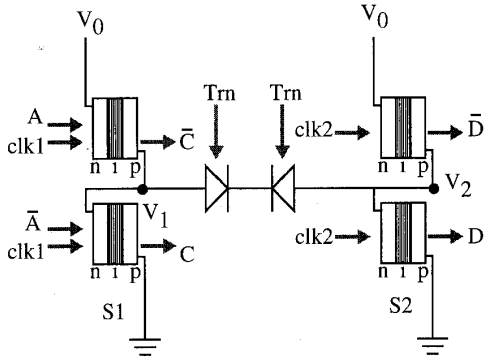

Fig. 12. Optoelectronic transmission gate connecting two S-SEED's. A and $\bar{A}$ represent the data; C and $\bar{C}$ represent the output from S-SEED $S1$; D and $\bar{D}$ represent the output from S-SEED $S2$; *Trn* represents the transfer beams that determine whether $D = A$. In the devices that we describe here, the transmission gate is made up of quantum-well p–i–n diodes.

lators. These modulators generated inputs A, B, C, and D. The other four modulators geneated the complements. The bottom trace shows one of the output beams. The output beam is only a logic "one" when *A and B* are logic ones *or* when *C and D* are logic "ones". The optical powers of the beams were ~ 27 μW. If we assume a 2 : 1 contrast ratio of the inputs and assume that all the power measured is contained within the eight beams, then the optical powers of each input were ~ 2.2 μW and ~ 1.1 μW for the high and low states, respectively. If we again define the required differential optical energy per beam as the difference in optical power of the pair of beams of a given input (1.1 μW times the switching time ~ 5 μs), the required differential optical energy per beam was equal to ~ 5.5 pJ.

L-SEED Optoelectronic Transmission Gates

The L-SEED concept can be extended to devices that implement multiplexers, demultiplexers, and shift registers as well as additional multiport logic gates by using optoelectronic transmission gates. These optoelectronic transmission gates consist of two back-to-back photodiodes and perform the function of a transmission gate in CMOS circuits [8]. Like their electronic counterparts, these devices electrically transfer the logic state from one device to another under external control, but in these devices the control is optical. An example of an optoelectronic transmission gate connecting two S-SEED's is shown in Fig. 12. By itself, this circuit only performs the function of an optoelectronic relay. However, this circuit is the fundamental building block of more sophisticated circuits that contain more than one transmission gate which we will discuss later.

In this circuit, inputs A and $\bar{A}$ set the state of S-SEED $S1$, clock beams *clk*1 and *clk*2 read the states of S-SEED's $S1$ and $S2$, and transfer beams *Trn*, determine whether the state of $S2$ is transferred to the state of $S1$. First we apply signal beams A and $\bar{A}$ to set the state of $S1$. There is a specific voltage V_1 on the center node of $S1$ that represents the logic state of $S1$. At the same time we apply transfer beams *Trn* to the optoelectronic transmission gate.

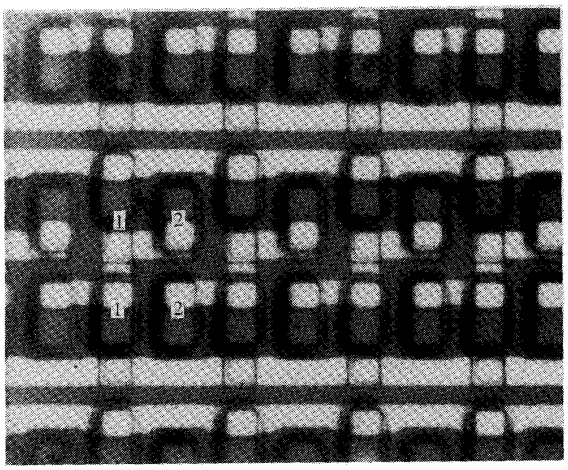

Fig. 13. Photograph of part of the S-SEED array with neighboring S-SEED's connected with optoelectronic transmission gates. The two diodes of a particular S-SEED and a particular transmission gate are oriented vertically. Diodes labeled "1" make up a S-SEED and diodes labeled "2" make up a transmission gate.

These beams effectively "short" $V2$ and $V1$ if the currents flowing in the optoelectronic transmission gate are greater than the dark currents flowing in $S2$. Therefore, signal beams A and $\bar{A}$ also determine V_2 and thus set the state of $S2$. If the transfer beams are not turned on, the state of $S2$ is not influenced by the state of $S1$, other than by the leakage currents and capacitive coupling of the transmission gate. After the states of $S1$ and $S2$ have been determined, clock beams *clk*1 or/and *clk*2 are turned on and the states of $S1$ and $S2$ can be read.

A 32 × 16 array of S-SEED's has been made with neighboring devices connected with these transmission gates. A photograph of a section of the array is shown in Fig. 13. All optical windows are 5 μm × 5 μm. In the horizontal direction, the S-SEED and transmission gate windows are interleaved. The center to center spacings of the S-SEED windows are 20 μm and the center to center spacings between transmission gate windows are also

20 μm. The center to center spacings between adjacent S-SEED and transmission gate windows are 10 μm.

Switching Nodes

To make a 2 × 1 photonic switching node, three S-SEED's and two of these optoelectronic transmission gates are connected as shown in Fig. 14. The location of the switching nodes can be optically configured by selecting the locations of the signal and clock beams. Switching nodes may be located on 60 μm × 40 μm centers for a 10 × 16 array of switching nodes, with a single transmission gate between nodes, or 80 μm × 40 μm centers for a 8 × 16 array of switching nodes, with two transmission gates and a spare S-SEED between nodes. The latter case may simplify the optical system because all data inputs (A to C to the next A, etc.) are on 40 μm centers.

In operation, first we apply the data inputs A, $\bar{A}$, C, and $\bar{C}$ and the control inputs B and D to the switching node and subsequently apply the clock beams *clk* which are modulated by $S2$ to give the output data E and $\bar{E}$. Control inputs B and D are complementary. If control input B is greater than control input D (i.e., $B = 1$ and $D = 0$), then V_2 will be equal to V_1 and output E will be equal to data input A. However, if control input B is less than control input D (i.e., $B = 0$ and $D = 1$), then V_2 will be equal to V_3 and output E will be equal to data input C.

For the node to function correctly, the larger of the signal beam powers of the selected input must be sufficiently greater than each of the control beam powers. Otherwise, the unselected input can influence the output state of the node. For example, suppose V_1, V_2 and V_3 are initially equal to ~ 0 V. Now, assume that data input A is a logic "one" ($A > \bar{A}$), data input C is a logic "zero" ($C < \bar{C}$), control input B is a logic "one" and control input D is a logic "zero" ($B > D$). If the switching node is operating correctly, output E should be equal to input A. Since the power of input A is greater than that of input $\bar{A}$, the top diode of S-SEED $S1$ will generate more photocurrent than the bottom diode of $S1$ and V_1 will "switch" to $\sim V_0$ V. However, there is an additional photocurrent flowing in the transmission gate connected to the center node of $S1$. Since the initial voltage V_2 on the other end of the transmission gate is ~ 0 V, the initial photocurrent flowing in the transmission gate effectively adds to the photocurrent flowing in the bottom diode of $S1$. If the initial photocurrent flowing in the top diode of $S1$ is not greater than the sum of initial photocurrents in the transmission gate and the bottom diode of $S1$, then V_1 will remain at ~ 0 V, and the state of $S1$ will be incorrect. Since the power of input C is less than that of $\bar{C}$, the top diode of S-SEED $S3$ will generate less photocurrent than the bottom diode of $S3$ and V_3 will also remain at ~ 0 V. Since, V_1 and V_3 remain at ~ 0 V, V_2 will also remain at ~ 0 V. Thus, output E will *not* be equal to input A.

In an initial experiment, a single 2 × 1 switching node was demonstrated. The data signals A, $\bar{A}$, C, and $\bar{C}$ and the control signals B and D were generated using differential quantum-well modulators. A 1 × 2 binary phase grating split each output from the control differential modulator (i.e., B and D) into the two beams that are required by the back to back diodes of the transmission gates. The beams incident on the differential modulators that generated the data signals were modulated with a 50% duty cycle to enable sequential operation. The beams incident on the differential modulator that provided the control beams were also modulated with a 50% duty cycle so that they would have the same temporal data format as the data inputs although the control signals did not need to be clocked. One differential modulator set input A to a "0 1 0 1" pattern and another set input C to a "0 0 1 1" pattern. Control input B was modulated with four "ones" followed by four "zeros" (and control input D was its complement). The control of the node therefore alternated from selecting input A to selecting input C every four bits. The output signal is shown in Fig. 15.

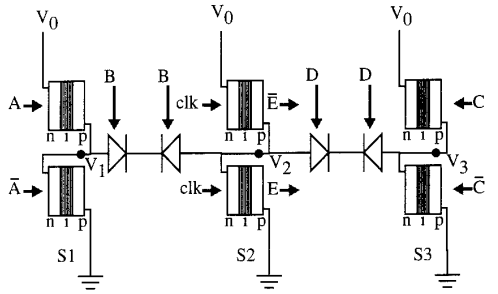

Fig. 14. Schematic diagram of part of the arry of Fig. 13 configured as a switching node. A and $\bar{A}$ represent one data input, C and $\bar{C}$ represent the second data input; B and D (which are complementary) represent the control input; E and $\bar{E}$ represent the data output.

The switching time is determined by the time it takes the photocurrents to charge the capacitances of the switching node. The control beam powers should be as large as possible so that there are large photocurrents to charge the capacitances of the transmission gate. However, if the control beam powers are too high, input S-SEED's $S1$ and/or $S3$ will switch too slowly or perhaps not switch at all. In our experiment the control beam powers were adjusted to about one half of the signal beam powers. The maximum speed of the switching node was ~ 1 μs, limited by the powers of the control beams. The node output was incorrect when the time that the signal beams were applied was reduced below ~ 1 μs. The control beam powers were ~ 760 nW and $\sim$ 1.5 μW for the "low" and "high" control beams, respectively. Thus, the required differential control beam energies were ~ 750 fJ. The signal beam powers were ~ 1.8 μW and ~ 3.6 μW and ~ 2.5 μW for the "low" and "high" states of inputs A and C, respectively. In this case the required signal optical energies were 1.3 and 1.8 pJ for the two inputs.

We have also tested an 8 × 16 array of 2 × 1 switching nodes operating concurrently using input data generated

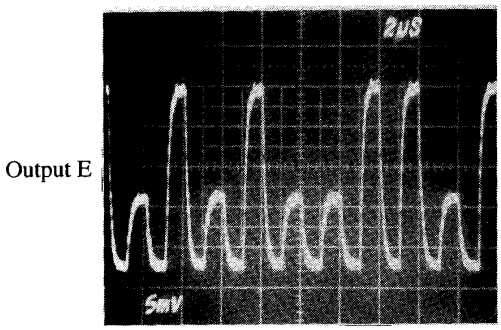

Fig. 15. Experimental results demonstrating operation of part of the array of Fig. 13 operated as a 2 × 1 switching node. (Input data signals were "0 1 0 1" and "0 0 1 1" and control alternated every four bits between inputs *A* and *C*.)

by a S-SEED array acting as a memory. The experimental setup is shown in [6] with the first S-SEED in that experiment used to generate the data and second S-SEED array in that experiment replaced by this array of 2 × 1 nodes. The S-SEED windows are oriented vertically. We will call the output a logic "one" when the top diode has greater reflectivity than the bottom one. The left half of the input S-SEED array was set to a logic "one" and the right half of the S-SEED array was set to a logic "zero". The outputs from a 4 × 8 section of this array are shown in Fig. 16(a). The outputs from this array were imaged onto the array of 2 × 1 switching nodes using a crossover interconnection network [14].

The input to the switching node array (output of the crossover interconnection network) consists of two overlapped images, one identical to the S-SEED output and one with a left to right reversal caused by a horizontal prism in the crossover network. The left S-SEED $S1$ in Fig. 14, of each 2 × 1 node had as logical input equal to the logical output of the S-SEED array (nonaltered image) as shown in Fig. 16(a), while the right S-SEED $S3$, of each 2 × 1 node had a logical input equal to the complement of the logical output from the S-SEED array (reversed image) as shown in Fig. 16(b). Therefore, each 2 × 1 switching node had one of its two data inputs as a logic "one" and the other of its data inputs as a logic "zero" [see Fig. 16(a) and (b)].

A single set of control beams was generated by passing the output of a laser diode through a 32 × 8 binary phase grating. The control signal selected either data input *A* or data input *C* by moving a mirror in the system to direct the control beams to their appropriate transmission gates. Since there was only a single set of control beams all nodes, although independent, were controlled similarly. The data outputs from the array of 2 × 1 switching nodes are shown in Fig. 16(c) and (d) for a 4 × 8 section of switching nodes. In these figures, there are eight columns of spots arranged in four groups of two. Recall that two diodes of a particular S-SEED are oriented vertically. In each figure four columns of spots represents the output beams and four columns of spots represent the control

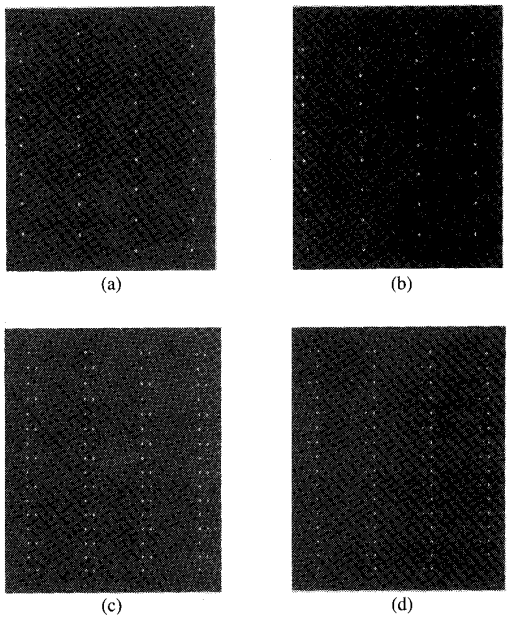

Fig. 16. Inputs and outputs from a 4 × 8 section of 2 × 1 switching nodes operating concurrently (a) inputs A and $\overline{A}$ for each device, (b) inputs C and $\overline{C}$ for each device, (c) output for $B = 1$ and $D = 0$ (input A selected), and (d) output for $B = 0$ and $D = 1$ (input C selected). In (c), control beams are shown in first, third, fifth, and seventh columns and output beams (E and $\overline{E}$) are shown in second, fourth, sixth, and eighth columns. In (d), control beams are shown in second, fourth, sixth, and eighth columns and output beams (E and $\overline{E}$) are shown in first, third, fifth, and seventh columns. The physical location of the output beams is the same in (c) and (d). Recall the S-SEED's are naturally inverting in that a "high" signal' incident on the top diode and a "low" signal incident on the botton diode will switch a device so that its corresponding output from the top diode is "low" and from the bottom diode is "high".

beams. The physical location of the output beams does not change, but the physical location of the control beams does change since they are directed to their appropriate transmission gates by moving a mirror. In Fig. 16(c), the first, third, fifth, and seventh columns are the control beams that are incident on transmission gates B to the left of the center S-SEED $S2$. In this case, the control beams selected input A. The second, fourth, sixth, and eighth columns are the output beam $\overline{E}$ and E. Since the S-SEED's are naturally inverting, the outputs from the top and bottom diodes of $S2$ in Fig. 14, are equal to the complements of the inputs to the top and bottom diodes of $S1$ in Fig. 14. In Fig. 16(d) the control beams selected input data C (i.e., $B = 0$, $D = 1$). In this figure, the second, fourth, sixth, and eighth columns are the control beams that are incident on the transmission gates, with control input D, to the right of the center S-SEED $S2$. The first, third, fifth, and seventh columns are the outputs of $\overline{E}$ and E. Again, the top and bottom outputs are inverted from the top and bottom inputs because of the inverting nature of the S-SEED's. For the 8 × 16 array of nodes, correct operation was observed for 124 out of 128 devices for both logic "ones" and logic "zeros" on each node input. The four devices that did not work correctly had debris on the device windows.

Extending the 2 × 1 switching node to n × 1 switching nodes can be done by having n input S-SEED's, n transmission gates and one output S-SEED. The required optical energy per input beam of the node would, in theory, be indedependent of the number of inputs, since the capacitance of only one input S-SEED, one transmission gate, and the output S-SEED needs to be charged by a single input. One could also build 2 × 2 switching nodes by starting with a 2 × 1 node and adding an extra set of two transmission gates connecting the center node of S-SEED's $S1$ and $S2$ to the center node of a second output S-SEED. We could extend this to n × m nodes where n is the number of inputs and m is the number of outputs. The required optical energy of each input would increase with the fanout of the electrical voltage of the input S-SEED for each input. However, networks constructed from larger node sizes would have fewer nodes, so although the optical energy required per node has increased, the total required optical energy may stay about the same. Node sizes the minimize the overall energy of a system for the integration of electronics with quantum-well modulators have been addressed [15], although the results do not apply directly to L-SEED's. The choice of an optimum node size depends on architectural and optical system design issues as well.

Multiplexers and Demultiplexers

A 2 × 1 switching node can also be used as a 2 × 1 multiplexer. As a multiplexer, first one input is selected and then the other. A timing diagram of a switching node operated as a multiplexer is shown in Fig. 17. The schematic diagram of Fig. 14 applies to the multiplexer. Data inputs A and C are applied out of phase with respect to each other. First, input A is applied. Control input B is applied concurrently with input A, so input A determines V_2 as well as V_1. During the second half of the data input cycle, a set of clock beams are applied to $S2$ providing output beams E and $\overline{E}$ that are logically equivalent to data input A. Then data input A and control input B are turned off and data input C and control input D are applied. Now, input C determines V_2 as well as V_3. During the second half of this data input cycle, the set of clock beams are applied to $S2$ providing output beams E and $\overline{E}$, which are now logically equivalent to data input C.

In our experimental demonstration, input data A, $\overline{A}$, C, and $\overline{C}$ were generated using two different quantum-well modulators. The clock beams incident on the A modulator were out of phase with respect to the clock beams incident on the C modulator. The control beams were generated by a third differential modulator. The light beams incident on this modulator were not modulated. The output clock beams were modulated at twice the data rate of input clocks. In this experiment the data inputs were "0 1 0 1" and "0 0 1 1". The multiplexer output is shown in Fig. 18. The required optical input power was about a factor of ten larger than it should have been based on the switching node experiment, probably because of misalignment

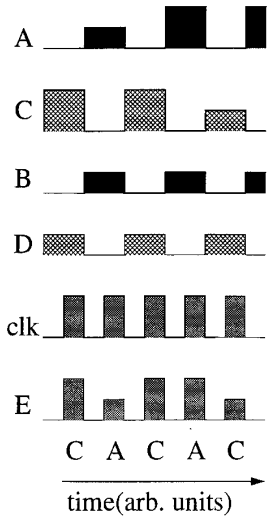

Fig. 17. Timing diagram of L-SEED 2 × 1 multiplexer. The schematic diagram for a 2 × 1 multiplexer is the same as for the 2 × 1 switching node and is shown in Fig. 14.

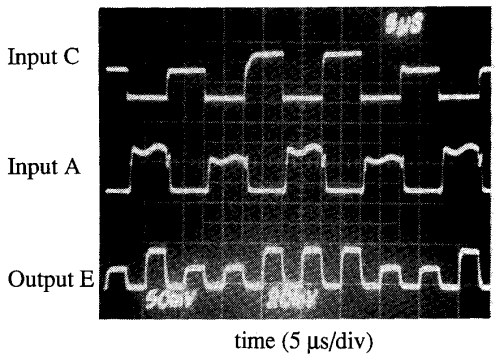

Fig. 18. Experimental results demonstrating operation of the second array as a 2 × 1 multiplexer. The top two traces represent the data inputs (A and C) and the bottom trace represents the output (E).

of the optical beams or perhaps because of the poor contrast ratio of one of the inputs (middle trace) in this experiment.

A 2 × 1 switching node can also be operated as a demultiplexer. A schematic diagram and a timing diagram of the demultiplexer are shown in Fig. 19. As a demultiplexer, first input beams E and $\overline{E}$ set the state of S-SEED $S2$. Concurrent with the application of the input beams, control beam B ensures V_1 is equal to V_2, setting the state of $S1$ equal to the state of $S2$. The clock beams $clk3$ are coincident in time with the signal beams E and $\overline{E}$ to ensure that $S3$ retains its state which is being read. Then, clock beams $clk2$ are appled to $S2$. The control beams and other clock beams that were on during the application of the signals remain on. It is not necessary to have a clock beam incident on $S2$; the signal beams could remain incident during this time. However, if we use clock beams, then the input and output from the demultiplexers have the

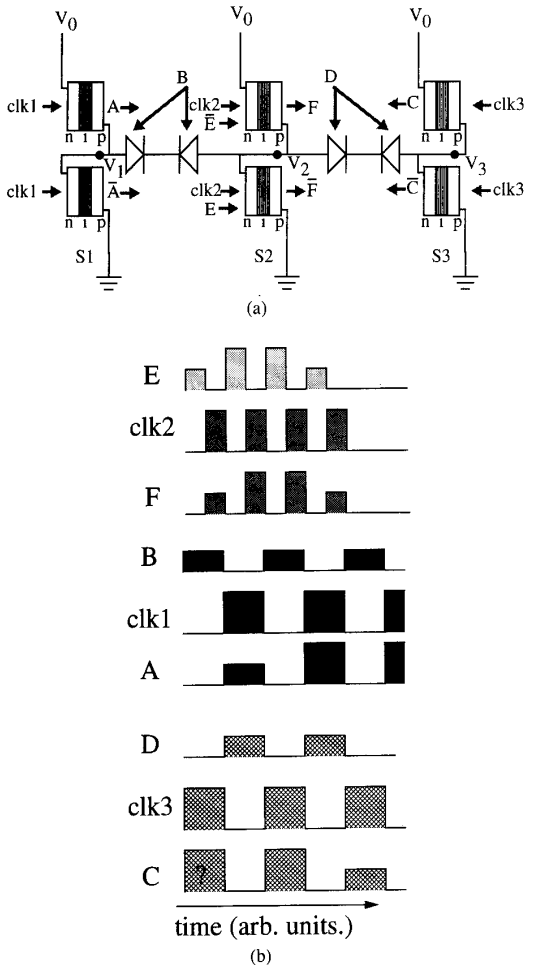

Fig. 19. L-SEED 2 × 1 demultiplexer. (a) Block diagram. (b) Timing diagram. E and $\bar{E}$ represent the data input; A and $\bar{A}$ represent one demultiplexed output; C and $\bar{C}$ represent the second demultiplexed output; and B and D represent the demultiplexer control signals.

same temporal data format so they (demultiplexers) can be cascaded. This set of clock beams also provides an output (with time-sequential gain) that is not demultiplexed as shown by F and $\bar{F}$ in Fig. 19. When clock beams $clk2$ are no longer on, the second bit of data E and $\bar{E}$ is incident on $S2$. Now, B becomes "low"and D becomes "high". Clock beams $clk1$, read out the first input data bit from $S1$ and ensure that the second bit of information now incident on $S2$ does not effect $S1$. Clock beams $clk3$ are now low so that the second bit of information now incident on $S2$ determines V_3. With the arrival of the third bit of information, B becomes "high", D becomes "low". Clock beams $clk3$ become "low", ensuring that V_1 is equal to V_2, and clock beams $clk3$ read out the second input data bit from $S3$.

A single 2 × 1 switching node was also tested as a demultiplexer. Two laser diodes generated the set of input beams E and $\bar{E}$ and third laser diode generated the clock beams $clk2$l incident on $S2$. A fourth laser diode generated control beams B and clock beams $clk3$ and a fifth laser diode generated control beams D and clock beams $clk1$. In the experiment, input beams E and $\bar{E}$ and clock beams $clk2$ were accidentally delayed by one-half bit period from the timing diagram in Fig. 19(b). Because of this, the data from the previous bit, destined for $S1$ for example, was first written to $S3$ during the time when $clk2$ is "on". Subsequently, data from the current bit, destined for $S3$, was correctly written to $S3$ during the application of the signal beams E and $\bar{E}$. Finally the current bit is read out by clock beams $clk3$. Timing in this manner still leads to correct operation of the gate, because that previous bit that was undesirably written to the incorrect output S-SEED is not read. Fig. 20 shows the undemultiplexed output F and demultiplexed outputs A and C. The data input was chosen so that when demultiplexed it would have outputs of "0 1 0 1" and "0 0 1 1". Correct operation of the device was observed.

Extending the 2 × 1 demultiplexer to n : 1 demultiplexers can be done simply by having n transmission gates connecting one input S-SEED to n output S-SEED's similarly to what was described for switching nodes. The effective capacitance that the input needs to charge would increase linearly with n, so the required optical energy of the device is also proportional to n. By cascading 2 × 1 demultiplexers, this problem is avoided at the expense of multiple stages. Also, in these experiments we demonstrated multiplexers and demultiplexers that interleave every bit of data. By the appropriate sequence of control signals, we could interleave words of any bit length. For example, the multiplexed data could consist of 8 bits from data input 1 followed by 8 bits from data input 2 and so on.

Optoelectronic Cascading L-SEED Shift Register

So far we have described applications of devices with transmission gates that *connected* S-SEED's, that is output node voltages were determined at the same time the inputs were applied. Another application of transmission gates is optolectronic *cascading* of devices where the inputs first set the state of one S-SEED, and subsequently the node voltage is transferred to a second S-SEED. An example of a sequential circuit is an optoelectronic shift register.

The array can be also configured as a shift register as shown in Fig. 21. First, the input signals set the state of the first S-SEED $S1$. Next, the clock beams $clk1$ and transfer beams $Trn1$ are applied simultaneously. The clock beams provide an optical output signal from $S1$ and hold the state of $S1$ while transfer beams $Trn1$ transfer that state electrically to $S2$. The power in the transfer beams must be sufficiently less than that of the clock beams to ensure that $S1$ retains its state. Otherwise, $V1$ will be influenced by $V2$ and $S1$ may lose its state. Then, clock beams $clk2$ and transfer beams $Trn2$ are applied to S-SEED $S2$ and transmission gate $T2$ to read the state of $S2$ and transfer the voltage on $S2$ to $S3$. Simultaneously,

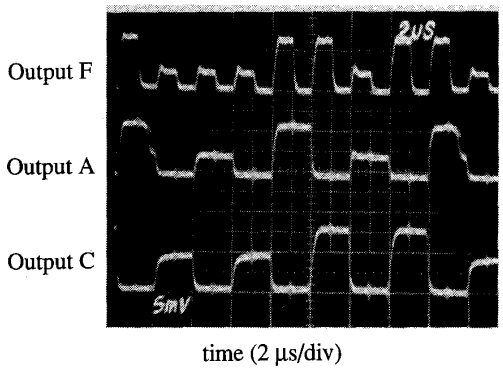

Fig. 20. Experimental results demonstrating operation of the second array as a 2 × 1 demultiplexer. The top trace represents the data input (undemultiplexed output) and the bottom two traces are the demultiplexed outputs.

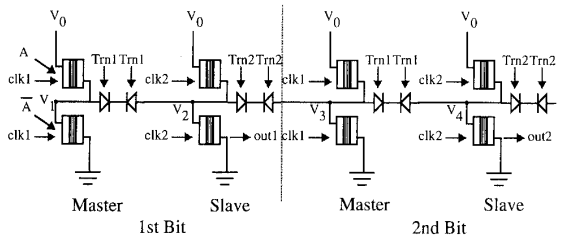

Fig. 21. Schematic diagram of part of the array in Fig. 13 configured as a shift register. A and $\bar{A}$ represent the data input; $clk1$ and $clk2$ represent the clock inputs; $Trn1$ and $Trn2$ represent the transfer beam inputs; and $Out1$ and $Out2$ are the outputs ($\overline{Out1}$ and $\overline{Out2}$ are not shown.)

the input signals are applied setting the new state of $S1$. Analogous to electronic shift registers, the odd numbered S-SEED's are called master flip-flops and the even numbered S-SEED's are called slave flip-flops. Because of the two-cycle nature of the clock beams, two S-SEED's (a master-slave flip-flop) holds one bit of information. Thus $2N$ S-SEED's implement a N bit shift register.

We demonstrated 2, 4, and 8 bit shift registers using part of the array. A pair of semiconductor laser diodes generated the complementary input data stream which consisted of a logic "one" followed by seven logic "zeros". Four additional semiconductor lasers provided the clock, transfer, complement clock, and complement transfer beams. Binary phase gratings produced either 2, 4 and 8 replicas of the input beams [16]. The parallel outputs from the second, fourth, sixth, and eighth bits of the eight bit optical shift register along with the data input are shown in Fig. 22.

One unique aspect of the shift register is that the transfer process is bidirectional, unlike electronic shift registers [8] or shift registers made by optically cascading S-SEED's [17]. We can transfer data from right to left by ensuring that transfer beams $Trn1$ are in phase with clock beams $clk2$ and transfer beams $Trn2$ are in phase with clock beams $clk1$. This is possible because S-SEED's are three terminal devices from an optical point of view, but the S-SEED is a *two-terminal* device from an electrical point of view, the two terminals being represented by the

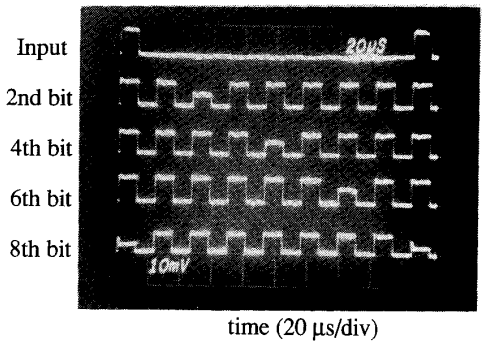

Fig. 22. Optical input and parallel outputs from the second, fourth, sixth, and eighth bits of the eight bit optical shift register.

center node voltage and either ground or V_0. The optoelectronic transmission gates are also two terminal devices, as are electronic transmission gates. In VLSI design, using a transmission gate to transfer the information from one logic gate to another is a unidirectional process, since the logic gates have good electrical input/output solution. However, *electrically*, the S-SEED's have no input/output isolation. If we ensure that the clock beams present on gate 1, for example, generate significantly more photocurrent than the transfer beams, gate 1 will retain its state during a transfer to gate 2, and thus the transfer of information occurs in one direction. Thus, the S-SEED combined with the transmission gate acts like a three terminal device in that there is sufficient input/output isolation, yet the particular transmission gate associated with a particular S-SEED can be optically programmed. Thus, the direction of information flow and the physical location of the inputs and outputs can be optically programmed as well.

For the two bit shift register, the optical powers in the transfer beams in the "on state" were $\sim 10\ \mu$W and $\sim 2.7\ \mu$W per beam for $Trn1$ and $Trn2$, respectively. The optical powers in the clock beams were 62 and 50 μW per beam for $clk1$ and $clk2$, respectively. The minumum switching time was ~ 660 ns at these powers. That is, correct operation was not observed when the signal beams were applied for less than ~ 660ns. The product of the switching time and the incident power gives the amount of energy that was supplied in each clock or transfer beam. The energies per beam required for operation were ~ 6.6 and ~ 1.7 pJ for the transfer beams and ~ 41 and $\sim$ 33 pJ for the clock beams. The 1.7 pJ required from the transfer beams is approximately what is expected based on our results for S-SEED's [4]. However, the clock beam energies were higher than expected. The primary reason for this is that the transfer beams must be sufficiently less than the clock beams so that S-SEED $S1$, for example, does not lose its state when the transfer beams are transferring its information to S-SEED $S2$. If the input contrast ratio at the edge of the bistable loop is $(1 + x)$, then the transfer beam powers should be at least $1/x$ times smaller than the clock beam powers. Otherwise, the photocurrent in the transmission gate will force $S1$ outside its bistable

region. The measured input contrast ratio at the edge of the bistable loop varied from ~1.12 at 848 nm to ~1.20 at 850 nm. Based on that measurement, the clock powers needed to be 5-8 times larger than the transfer beam powers. For our experiment, the clock beam powers were ~4 and ~20 times greater than the transfer beam powers. If we allow a factor of two or so because of misalignments in our system, then the results are reasonable. The required optical energies per clock beam in this experiment of ~41 and ~33 pJ were comparable to that required in optically cascaded S-SEED's of ~20 pJ [18]. However, if we could build devices with a 2:1 required input contrast ratio at the edge of the bistable loop, the energy in the clock beams would be at most a factor of two higher than that of the transfer beams, and we would expect the required energy to be less than ~3.5 pJ per clock beam. In this case, *optoelectronically* cascaded S-SEED's (i.e., this shift register) may be slightly more energy efficient than *optically* cascaded S-SEED's.

The switching times of S-SEED's have been measured as ~33 ps using mode locked pulses [19]. The switching time of the device in that experiment was limited by the time it takes the carriers to escape from the quantum wells. The *RC* time constant of the devices from the ohmic contact resistances was ~5 ps [19], the charging time of the capacitance from the photocurrent was ~2 ps [19], and the "response time" of the quantum confined Stark effect is estimated to be ~100 fs [20]. We would expect the switching times of logic SEED's to be similar because the physical mechanisms that govern the operation of the devices and the device fabrication are the same. The switching times of the devices *in a system* are generally limited by the charging time of the device capacitance with the photocurrent. This photocurrent is directly proportional to the optical power of the input beams which are derived from the outputs of one or more other devices after passing through some interconnection optics. The optical powers of these input beams are limited by saturation of the absorption of the quantum-well material in the device whose state is being read and by the losses of the devices and the interconnection optics between the devices. A photonic ring counter has been made by cascading two S-SEED's that has a switching time of 40 ns when the devices are operated conventionally and 10 ns when the devices are operated as signal sense amplifiers [18]. We would expect switching times of L-SEED's in systems to be slightly higher because the required optical switching energies of L-SEED's are slightly higher. We have not yet reached a fundamental limit because the absorption losses of the devices could be reduced, the losses of the optical system could be reduced, the required electric field change of the devices is going from one state to another could be reduced, and perhaps the devices could be made smaller.

For optoelectronically cascaded L-SEED's, the switching time in a system could be significantly faster. The switching time will again be limited by the charging times of the capacitances of the device; this time will be limited, for the case of the shift register, by the powers in the transfer and clock beams. Since the clock and transfer beams were not derived from the outputs of the other devices, they could have significantly more power than the signal beams in optically cascaded devices. Thus, we would expect the shift register to operate faster than systems consisting of optically cascaded devices. In fact, it may be possible to use short pulses to get switching times to the shift register much less than 1 ns. However, at repetition rates above 1 GHz, average optical powers greater than 1 mW are required for required optical energies of ~1pJ. For large arrays of devices operating at these powers, heating may be a problem. Because the physical mechanisms (the escape time of carriers from the wells and the response time of the material) that limit the intrinsic speeds of the devices are fast, the key to making L-SEED's (and any SEED's for that matter) operate at high bit rates in systems is to reduce the absorptive losses of the devices and of the optical system and reduce the required optical and electrical energies as much as possible.

Conclusion

In conclusion, we have demonstrated two-dimensional arrays of logic self-electrooptic effect devices (L-SEED's), consisting of electrically connected quantum-well p-i-n diode detectors and modulators,. The electrical connections between the detectors resemble those interconnecting transistors in CMOS circuits. Like the S-SEED's, the devices have gain without critical biasing, timing regeneration, and logic level restoration and wavefront quality restoration. We have shown that each element in a 16 × 16 L-SEED array can implement any of the four basic boolean logic functions without the use of a preset beam. Each element in a 4 × 4 L-SEED array can implement the function $E = AB + CD$. This function is especially useful for exclusive OR gates and 2 × 1 photonic switching nodes. We extended the L-SEED concept to SEED's containing optoelectronic transmission gates. We have built and tested a 32 × 16 array of symmetric SEED's (S-SEED's) connected with these transmission gates. The array can be configured as an array of 2 × 1 switching nodes, multiplexers, demultiplexers or shift registers. Individual switching nodes, multiplexers and demultiplexers were demonstrated, an 8 × 16 array of 2 × 1 switching nodes was operated concurrently, and an eight bit shift register was demonstrated.

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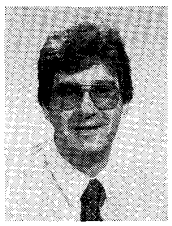

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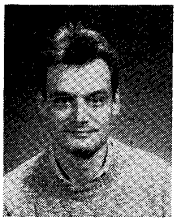

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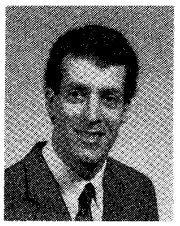

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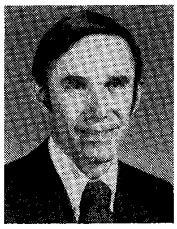

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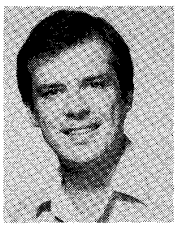

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