Optical logic using electrically connected quantum well PIN diode modulators and detectors

Anthony L. Lentine, David A. B. Miller, J. E. Henry, J. E. Cunningham, L. M. F. Chirovsky, and L. A. D'Asaro

We present new optoelectronic logic devices or circuits consisting of electrically connected quantum well PIN diodes capable of implementing any boolean logic function. One class of circuits uses single beams to represent the logic levels and compares their intensities to a locally generated reference signal. A second class of circuits routes signals as differential pairs. The connections of diodes in these circuits resemble the transistor connections in NMOS and CMOS logic families. We demonstrate simple optical programmable logic arrays (e.g., $E = AB + CD$) using both of these classes of circuits.

I. Introduction

Many types of logic devices have been proposed for optical computing and photonic switching.[1,2] All of these must have the required gain for cascading devices and at least a minimum functionality needed to perform general Boolean logic functions by optically interconnecting these devices (for example, a NOR gate is sufficient). It is clearly preferable, from the point of view of trying to build optical computing or photonic switching systems, that the devices are physically sufficiently functional to be easy to use. For example, a three-terminal device is clearly preferable to a two-terminal device because the input/output isolation present in three-terminal devices helps remove the problem of critical biasing present in two-terminal devices. It is also advantageous that there is some choice in logical functionality. Although it is possible to construct an arbitrary optical computer from two input NOR gates alone, a more optimal architecture may be constructed if more complex gates are available. Finally, it is important that the devices operate at fast speeds with low power requirements. Self-electrooptic effect devices (SEEDs)[2] offer the promise of satisfying all these requirements. SEEDs rely on changes in the optical absorption that can be induced by changes in an electric field applied perpendicular to the thin semiconductor layers in multiple quantum well material.[3] Typically these quantum wells are contained in the intrinsic region of a reverse biased PIN diode. When combined with an appropriate electrical circuit (i.e., load), the resultant device can have optoelectronic feedback and bistability. Since the first demonstration of a simple resistor-biased SEED,[4] much of the subsequent effort has concentrated on enhancing the functionality of the devices. More functionality can be achieved in SEEDs by having more than one light beam incident on several PIN diodes. For example, by replacing the resistive load with a photodiode that was illuminated by a visible (λ = 633-nm) beam, a diode biased SEED[5,6] (D-SEED) could be operated over many decades in power by adjusting the light input on the photodiode. The beam incident on the photodiode could also control the light output from the quantum well diode, and this device could act as a memory that could hold its state for up to 30 s when both the visible and infrared beams were removed.[6] A second example, the symmetric SEED (S-SEED),[7] consists of two quantum well PIN diodes electrically connected in series. It has time-sequential gain, provides for signal timing regeneration, is insensitive to optical power supply fluctuations, and provides effective input/output isolation. Because the signal inputs and outputs are differential in nature, specific logic power levels need not be defined and operation of the device is possible over a power range spanning several decades. Thus, the S-SEED satisfies the most basic requirement that it be easy to use. It also has good logical functionality in that it can act either as an optical set reset latch or as a differential logic gate capable of NOR, OR, NAND, and AND functions.[8] Additionally, arrays of S-SEEDs

All authors are with AT&T Bell Laboratories: A. L. Lentine is at Naperville, Illinois 60566; L. M. F. Chirovsky and L. A. D'Asaro are at Murray Hill, New Jersey 07974; and the other authors are at Homdel, New Jersey 07733.

Received 4 June 1989.
0003-6935/90/142153-11$02.00/0.

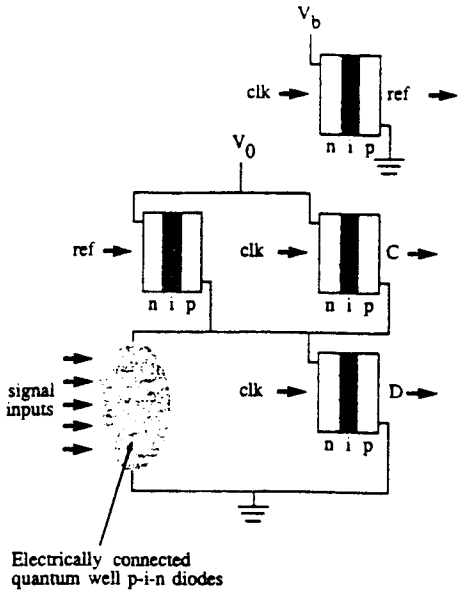

Fig. 1. Single ended logic gate. Output C is the noninverting (i.e., ORs and ANDs) output and output D is the inverting output. An extra quantum well PIN diode connected to a voltage source supplies the reference beam to the next stage of devices.

have been made[9] that have 3-pJ switching energies and subnanosecond switching speeds (with slightly higher energies).[10] We can attain more functionality by extending the S-SEED concept to more than two diodes in series to get multistate self-electrooptic effect devices[11] (M-SEEDs) that can behave as optically enabled S-SEEDs, select the least intense of many input signals, or act as image thresholding devices.

In this paper we describe and demonstrate a novel class of SEEDs, which are extensions of M-SEEDs, consisting of electrically connected quantum well PIN diodes. These devices or circuits can perform any Boolean logic function while retaining good physical functionality in that the devices are easy to use. The circuits may be considered as functional units, sometimes referred to as smart pixels,[12] that are interconnected with light beams propagating perpendicular to the plane of the circuits, although in principle integrated optics (i.e., waveguides) may be used for interconnections as well. The logic function is realized by the photocurrents changing the voltage across the quantum well diodes. Therefore, these circuits fall under the classification of SEEDs.[13] Two classes of circuits are discussed. The first class of circuits, which we will refer to as single ended logic circuits, has configurations of quantum well diodes that are quite similar to transistor configurations in NMOS.[14] In optical systems using these circuits, the optical signals are routed individually and compared to a locally generated reference beam. If the reference beam is generated using the same laser that supplies the signal beams, we avoid the critical biasing common to most optical bistable devices and have time-sequential gain, good input/output isolation, and signal retiming. In addition, we can define logic levels relative to the reference beam power level and operate the devices (circuits) over a power range of several decades as well.

In optical systems using the second class of circuits, we route the signals as differential pairs. These circuits have diode connections similar to transistor connections in CMOS.[14] They also avoid critical biasing, have time-sequential gain, good input/output isolation, and signal retiming. These circuits are more complex than the first class but they do not require a reference beam to be generated. Therefore, optical systems using these circuits may be easier to build than the comparable systems using the single ended circuits.

The rest of the paper is organized as follows. In Sec. II we describe the properties and operation of the single ended logic family. Then, we describe the basic OR/NOR and NAND/AND functions and show how to make more complex functions. We show two examples of more complex functions and show experimental results of a circuit implementing $E = AB + CD$. In Sec. III we describe the differential logic family and also show experimental results of a differential circuit implementing the same logic function.

II. Single Ended Family

Figure 1 shows the class of single ended logic gates that we describe. Although in many cases the same quantum well PIN diodes can be used for the detection and modulation processes, for simplicity, the circuits that we present have one set of several diodes on which the input signals are incident (signal diodes), one diode on which the reference beam is incident (reference diode), and a set of two diodes that generates the output beams from a set of incident equal power clock beams (output S-SEED). Any two (or N) parallel connected diodes may be replaced by a single diode with an optical window large enough for two (or N) beams. The descriptions of the circuits use only quntum well PIN diodes, but in fact, it is not absolutely necessary that the diodes with the incident input beams have quantum wells, although better switching may result if they do. This better switching behavior results from the increase in absorption of the quantum well diode with reducing voltage; this change in absorption tends to further enhance the difference in photocurrent between the diodes, hence switching them faster. The devices are operated by setting the state of the device using relatively low power input signal and reference beams and, subsequently, reading out the state using a pair of equal high power clock beams, achieving the same time-sequential gain mechanism that is present in the S-SEED.

The operation of the logic gate is described below. First, the signal beams and reference beams are applied to the respective diodes. The reference beam may be provided by passing a previous clock beam through a quantum well modulator with a fixed voltage on it. In this case, the reference beam and signal beams are not only derived from the same (clock) laser, but also pass through quantum well PIN diodes with the same characteristics, further reducing the need for

critical biasing. The voltage that will be present on the node between the signal diodes and the reference diode will be a function of the currents generated by these diodes. For noninverting functions (i.e., combinations of ANDs and ORs), we adjust the reference beam power level so that the voltage across the reference diode will be essentially zero, if the logic function is not satisfied. This will occur if the photocurrent generated by the reference diode is initially greater than that generated by the signal diodes. At the same time, we adjust the reference beam power level so that the voltage across the reference diode is essentially equal to the supply voltage if the logic function is satisfied. In this case, the photocurrent generated by the reference diode must be initially less than that generated by the signal diodes. These two cases give us a range of power levels for the reference beam, so there is no critical biasing. If we are using quantum well PIN diodes for these detectors, there is a range of input power levels where bistability exists. Therefore, we must be sure in the two cases given above that the photocurrent generated in the reference diode is sufficiently greater or less than that generated by the signal diodes so that the resultant voltage across the reference diode is uniquely defined (i.e., outside the bistable loop) for all sets of input signals. An alternative is to ramp the supply voltage up from zero during the application of the input signals and reference beam, effectively removing any bistable characteristics. Using photodetectors without a negative resistance region (for example, detectors without quantum wells) for the diodes with incident input signals also removes the bistable characteristics.

Since the center node of the output S-SEED is tied to the point between the reference diode and the signal diodes, once the voltage at this point has been determined (i.e., after the switching time of the circuit), we can remove the signal beams and apply the higher power clock beams to read out the state of the device at higher power, thus achieving time-sequential gain. However, bistability is required to read the state of the device, so we assume that the output S-SEED has a bistable region when applying the clock signals. To ensure this, we will describe the circuits operating at a wavelength where there is more absorption at low voltages than at high voltages, ensuring a region of bistability. Thus, for our discussion, low voltage means low optical output and high voltage means high optical output. Output signal C in Fig. 1, will be a noninverting output (high when the logic function is satisfied), because, as we stated above, the voltage across the reference diode will be essentially equal to the power supply voltage when the logic function is satisfied. Since output D is complementary to output C, it will be the inverting output (for example, output D is used for NOR and NAND gates). It is possible to operate at wavelengths where there is no bistability in the S-SEED, for example, at longer wavelengths where absorption increases with increasing voltage, but then there is no gain mechanism. Using phototransistors for the detector diodes, as proposed for transistor biased SEEDs (T-SEEDs),[13,15] could provide this gain mechanism and perhaps make a more energy efficient logic gate as well.

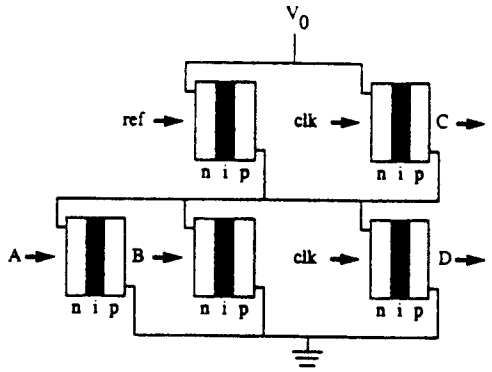

Fig. 2. Single ended OR/NOR gate: $C = A + B$; $D = \overline{A + B}$.

The signal diodes for the OR/NOR gate shown in Fig. 2 consist of two parallel connected quantum well diodes with input signals A and B. For OR operation, if either of the signals is a logic one the output should be a logic one; otherwise the output is a logic zero. The constraint on the reference beam power is described below. Assuming equal responsivity for all diodes, if the sum of the powers of the two input signals is sufficiently less than the reference beam power when both inputs are logic zeros, essentially 0 V will be present across the reference diode. Because the top diode of the output S-SEED is connected in parallel with the reference diode, output C will be low when the clocks are applied. Conversely, if the sum of the powers of the two input signals is sufficiently greater than the reference beam power when at least one input is a logic one, essentially the supply voltage will appear across the reference diode, and output C will be high when the clocks are applied. As mentioned above, we can remove the bistable characteristics during the application of the signals by momentarily turning off the dc power supply,[11] so that the device acts as a true optical comparator (thus, removing the term sufficiently from the above description). It follows directly from the two cases given above that the reference beam power must be between twice the power of a logic zero and the sum of the power of a logic zero and a logic one.

Since output D is complementary to output C, D is the NOR of A and B. An AND/NAND gate can be made using the same device by choosing the reference beam power between the sum of the power of a logic zero and a logic one and twice the power of a logic one. A logic gate whose output is a logic one when M of N inputs are high can be made by connecting N diodes, each with one input, in parallel. The range of reference beam power levels for this logic gate is given by

$$(M-1)P_{\mathrm{LOGIC1}} + (N-M+1)P_{\mathrm{LOGIC0}} < P_{\mathrm{REFERENCE}} < (M)P_{\mathrm{LOGIC1}} + (N-M)P_{\mathrm{LOGIC0}},$$

where $M = 1$ for an OR/NOR gate, $M = N$ for an AND/NAND gate, and $M = N = 1$ for an inverter/buffer or D-flip-flop. The optimum value for the reference beam

may be chosen in the middle of the two edges of the inequality. In this case, the reference beam amplitude is given by

$$P_{\text{REFERENCE}} = [(2M - 1)P_{\text{LOGIC1}} + (2N - 2M + 1)P_{\text{LOGIC0}}]/2$$

Since the constraints on the reference beam power become tight for large N, this logic gate is most useful for a small number of inputs.

Another AND/NAND gate shown in Fig. 3 is especially useful when combining OR/NOR and NAND/AND functions. The signal inputs, A and B, are incident on two serially connected diodes. Including the reference signal, the inputs are, thus, incident on three serially connected quantum well PIN diodes. For equal power input light beams, this device has three states, each state corresponding to one PIN diode having essentially the supply voltage across it (and higher optical output) and the other two diodes having essentially 0 V across them (see Ref. 11 for a discussion of the stable states of several quantum well diodes connected in series). If we ramp the voltage up from zero while applying the input signals (effectively removing any bistable characteristics), the diode with the least incident optical power has essentially the supply voltage across it. Otherwise, a particular diode must have input signals with sufficiently less power than the other two to uniquely determine the device state (i.e., fall outside the bistable regions). In operation as an AND gate, the output should be a logic one only if both inputs are logic ones; otherwise the output should be a logic zero. Assuming the reference beam power is greater than that of a logic zero, if either of signals A or B are logic zeros, the particular diode with the logic zero input will have essentially the supply voltage across it and the others (including the reference diode) will have essentially 0 V across them. If both signals are logic zeros, the diode with the input logic zero with the least power (assuming some small inequity exists) will have essentially the supply voltage across it, and the reference diode will still have essentially 0 V across it. Because the top diode of the output S-SEED is connected in parallel with the reference diode, when we apply the clock beams, output C will be low. If we also assume that the reference beam power is less than that of a logic one, if inputs A and B are both logic ones, the reference diode will have the least incident power and essentially the supply voltage across it. Therefore, when the clocks are applied, output C will be high. Thus, if the reference beam power is between a logic zero and a logic one, this circuit performs an AND function. Since the two outputs of the S-SEED are complementary, output D will be the NAND of the two inputs A and B.

An N input AND/NAND gate can be realized by connecting N diodes, each with one of the N incident signal beams, in series with the reference diode. The constraint on the reference beam power level for this gate is still that the power level in the reference beam is between a logic zero power level and logic one level (assuming no bistable loop). In this case, the multiinput AND/NAND gate has the same signal tolerances,

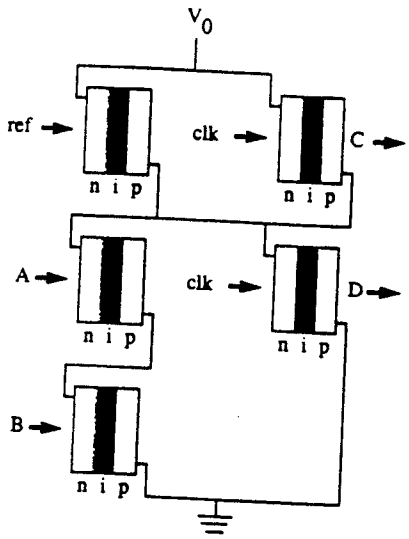

Fig. 3. Single ended AND/NAND gate: $C = AB$; $D = \overline{AB}$.

regardless of the number of inputs, and it can be easily shown that it also has the same switching energy. Thus, this N input AND/NAND gate is useful for large fan-ins. One practical constraint that may limit operation for very large N is the finite forward voltage that appears across the diodes that are in the low state (i.e., they are photovoltaic). The presence of this voltage does not alter the basic function of the device, but the sum of all these forward voltages must not be so large as to cause breakdown in the diode in the high state. The diodes used in our experiments have forward voltages of ~1 V and breakdown voltages >40 V, so this would limit us to approximately forty inputs.

Now let us consider how to implement arbitrary functions. Figure 4(a) shows that to implement the OR of two subfunctions, we merely connect the circuits performing the subfunctions in parallel. Figure 4(b) shows that to implement the AND of two subfunctions, we merely connect the circuits performing the subfunctions in series. One example of such a function is $E = AB + CD$. The circuit for implementing this function is shown in Fig. 5. Note that we have now combined the reference diode and the top diode of the output S-SEED into one diode. Subgroup 1, consisting of two PIN diodes connected electrically in series, performs the AND of A and B. Subgroup 2, also consisting of two diodes in series, performs the AND of C and D. By connecting subgroups 1 and 2 in parallel, the circuit performs the desired OR of AB and CD. We can generalize this circuit to include p parallel connected groups of s_p series diodes, where each group of serially connected diodes need not have the same number of diodes to realize a programmable logic array. (i.e., the ORs of many ANDs).

Let us consider another arbitrary function given by $E = (AB + C)D$, implemented by the circuit shown in Fig. 6. First, AB is implemented with serially connected diodes. A diode in parallel with this serial group performs the OR of AB and C. We call these three diodes subgroup 1. An additional diode is connected

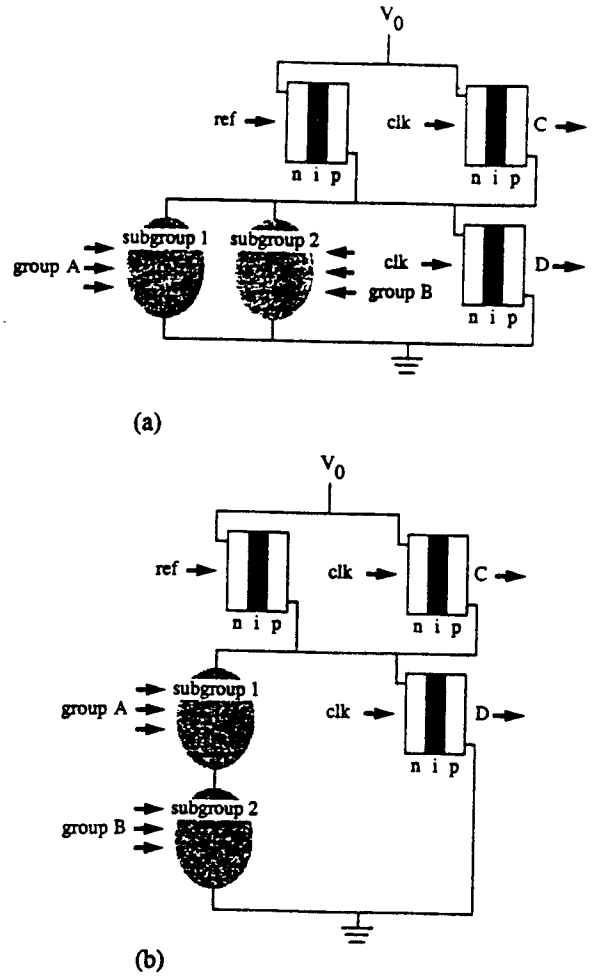

Fig. 4. Combinations of subfunctions implemented with single ended logic gates: (a). (C = subfunction 1 + subfunction 2, D = $\overline{\text{subfunction 1 + subfunction 2}}$); (b). ($C$ = subfunction 1 · subfunction 2, D = $\overline{\text{subfunction 1 · subfunction 2}}$).

in series with subgroup 1 to perform the AND function of ($AB + C$) and D. Then these diodes are connected in series with the reference diode to provide the output voltage that feeds the center node of the output S-SEED.

In the circuit above, the contrast ratio of the input signals must be greater than 2:1 for the logic gate to function properly. This is because a logic one for input beam D must generate more current than logic zeros on input beams A, B, and C. Since the diode with incident beam C is connected in parallel with the set of diodes with incident beams A and B, the contribution of the currents of any one of these three diodes is twice that of the diode with input beam D. In electronic circuits, the transistors may have different sizes to equalize these currents and make the gate operate optimally. In optics, the current generated is independent of device size, so instead, optical attenuators may be added to achieve optimum performance, particularly when the input signals have small contrast ratios between the two logic levels. The optical attenuators will be different for each diode, so they may either be fabricated as part of the devices or may be a

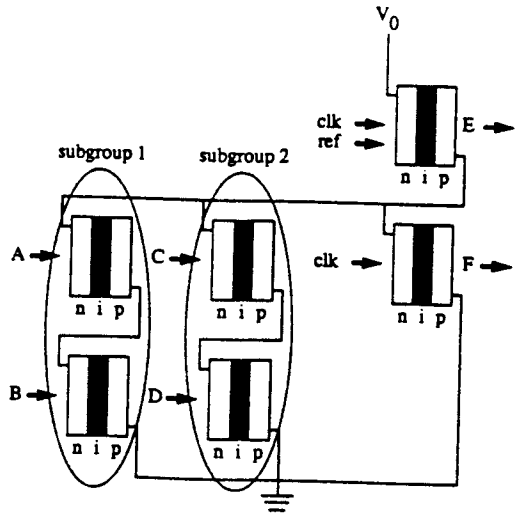

Fig. 5. Single ended logic gate implementing $E = AB + CD$. The circles indicate the S-SEEDs used in the experiments.

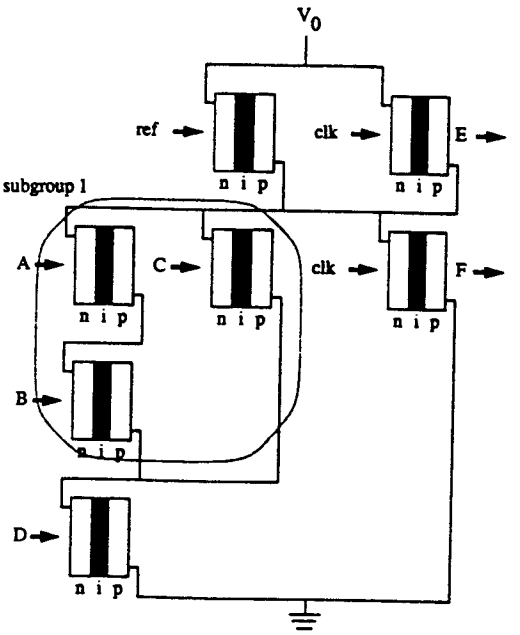

Fig. 6. Single ended logic gate implementing $E = (AB + C)D$. For the gate to operate at contrast ratios less than 2:1, input A, B, and C must be attenuated by 50%.

patterned array of attenuators placed in the image plane of the device. This second approach has been suggested for use with the symmetric SEED to minimize the effects of optical power level nonuniformities when performing logic functions.[16] Small arrays of patterned reflectors or mirrors have been demonstrated for combining optical beams incident on the devices[17] and these additional attenuators may be placed in the same patterned array. Again, if the input contrast ratio is sufficient (this is dependent on the particular circuit), the attenuators are not needed. However, we show how to calculate the appropriate values of the attenuators under the assumption that we want the logic gate to operate for contrast ratios greater than

one, which also minimizes the effects of optical power level nonuniformities for greater contrast ratios. Also, the values that we calculate may not be the optimum values for fastest speed of the logic gate.

The method that we use to calculate the optimum values for the attenuators is to choose those values that would allow the system to be in a perfect unstable equilibrium. In such a situation, the system is most sensitive to any slight perturbation of the inputs that would lead to switching. Therefore, assume that, with equal power incident beams and all diodes having the same responsivity, we wish to generate equal currents for all diodes; all diodes in the circuit are considered to be biased at an unstable equilibrium point, and only one such point will exist so that this is true for all diodes. Indeed, the device will be in such a state, provided the voltage is ramped up from zero while the signals are applied; otherwise, the bistability in the system will prevent this from happening. To illustrate this method of calculating the values for the attenuators, we use the example in Fig. 6. First consider the current generated by the diodes in subgroup 1. If equal currents are generated by each diode, the series current in subgroup 1 is twice that of the diode with input beam D. Therefore, the input signals incident on the diodes in subgroup 1 need to be attenuated by 50%. Although this is a simple example, this technique applies to more complex circuits as well.

Equally important is how to calculate the constraints on the reference beam power in one of these arbitrary circuits. In general, one has to write out the truth table for the circuit and calculate the contribution of each diode to the overall current in the circuit. Again, we assume that all diodes have the same responsivity. The contribution of serially connected subgroups is equal to the minimum of the subgroups, and the contribution of parallel connected subgroups is equal to the sum of the currents in each subgroup. Then one must find the largest of the currents where the function is a logic zero and the smallest of the currents where the function is a logic one. Assuming no bistability while the input signals are applied, the reference beam should generate a current between these two currents. Otherwise, the reference beam is constrained such that the ratio of the current generated by the signal diodes to the current generated by the reference diode, in the case where the function is satisfied, exceeds some critical factor k required to uniquely determine the state of the device. Conversely, the ratio of the current generated by the signal diodes to the current generated by the reference diode, in the case where the function is not satisfied, must be $<1/k$. It is possible that, for some circuits, both of these conditions cannot be met unless the input signals have sufficient contrast ratio or, as we stated above, the bistability is removed during the application of the signals.

The truth table and the currents generated for the circuit in Fig. 6 are shown in Table I. The currents calculated assume that input beams A, B, and C are attenuated by 50%, the responsivity is chosen for simplicity to be a constant value of 1 A/W, and the bistability is removed during the application of the input signals. (All currents scale with responsivity, which, although not constant, averages about 0.3 A/W from 0–15 V for one of these quantum well diodes.) From the last column in Table I, the constraints on the reference beam power level are:

$$P_{\mathrm{LOGIC0}} < P_{\mathrm{REFERENCE}} < 0.5(P_{\mathrm{LOGIC1}} + P_{\mathrm{LOGIC0}}).$$

The optimum power level for the reference beam is halfway between the two sides of the inequality. In this case, the reference beam power level is equal to $(1/4)P_{\mathrm{LOGIC1}} + (3/4)P_{\mathrm{LOGIC0}}$.

Table II shows the truth table for the circuit in Fig. 5. No attenuators are needed in this circuit. From the last column in Table II, the constraints on the reference beam power level are $2P_{\mathrm{LOGIC0}} < P_{\mathrm{REFERENCE}} < P_{\mathrm{LOGIC1}} + P_{\mathrm{LOGIC0}}$. Choosing a reference beam power halfway between the two sides of the inequality gives us a reference beam power level of $(1/2)P_{\mathrm{LOGIC1}} + (3/2)P_{\mathrm{LOGIC0}}$.

To demonstrate the functionality of this class of circuits, the circuit in Fig. 5 was demonstrated using three electrically connected S-SEEDs. The signal diodes were a 2×1 array of reflection mode devices[9] with 5×10-μm optical windows on 50-μm centers. These were electrically connected using coaxial cable to the output S-SEED which was a transmissive device[7] where an external connection could be made to the

Table I. Truth table for $E = (AB + C)D$, calculated currents levels assume signals A, B, and C are attenuated by 50% and a responsivity of 1 A/W

D	C	B	A	E	i_A	i_B	i_{AB}	i_C	i_{AB+C}	i_D	$i_{(AB+C)D}$
0	0	0	0	0	$.5P_0$	$.5P_0$	$.5P_0$	$.5P_0$	P_0	P_0	P_0
0	0	0	1	0	$.5P_1$	$.5P_0$	$.5P_0$	$.5P_0$	P_0	P_0	P_0
0	0	1	0	0	$.5P_0$	$.5P_1$	$.5P_0$	$.5P_0$	P_0	P_0	P_0
0	0	1	1	0	$.5P_1$	$.5P_1$	$.5P_1$	$.5P_0$	$.5(P_0+P_1)$	P_0	P_0
0	1	0	0	0	$.5P_0$	$.5P_0$	$.5P_0$	$.5P_1$	$.5(P_0+P_1)$	P_0	P_0
0	1	0	1	0	$.5P_1$	$.5P_0$	$.5P_0$	$.5P_1$	$.5(P_0+P_1)$	P_0	P_0
0	1	1	0	0	$.5P_0$	$.5P_1$	$.5P_0$	$.5P_1$	$.5(P_0+P_1)$	P_0	P_0
0	1	1	1	0	$.5P_1$	$.5P_1$	$.5P_1$	$.5P_1$	P_1	P_0	P_0
1	0	0	0	0	$.5P_0$	$.5P_0$	$.5P_0$	$.5P_0$	P_0	P_1	P_0
1	0	0	1	0	$.5P_1$	$.5P_0$	$.5P_0$	$.5P_0$	P_0	P_1	P_0
1	0	1	0	0	$.5P_0$	$.5P_1$	$.5P_0$	$.5P_0$	P_0	P_1	P_0
1	0	1	1	1	$.5P_1$	$.5P_1$	$.5P_1$	$.5P_0$	$.5(P_0+P_1)$	P_1	$.5(P_0+P_1)$
1	1	0	0	1	$.5P_0$	$.5P_0$	$.5P_0$	$.5P_1$	$.5(P_0+P_1)$	P_1	$.5(P_0+P_1)$
1	1	0	1	1	$.5P_1$	$.5P_0$	$.5P_0$	$.5P_1$	$.5(P_0+P_1)$	P_1	$.5(P_0+P_1)$
1	1	1	0	1	$.5P_0$	$.5P_1$	$.5P_0$	$.5P_1$	$.5(P_0+P_1)$	P_1	$.5(P_0+P_1)$
1	1	1	1	1	$.5P_1$	$.5P_1$	$.5P_1$	$.5P_1$	P_1	P_1	P_1

center node. Six AlGaAs semiconductor laser diodes provided the four signal inputs, reference beam input, and clock beams. The laser diodes were current modulated using a digital word generator. Figure 7 shows the four input signals and noninverting output signal. The output signal has the correct logic values as shown in Table II. No attempt was made to measure the switching energies of the devices, because of the added cables between the two halves of the circuit. In addition, the contrast ratio of the inputs was quite high (~100:1), whereas in an actual system, the input contrast ratios would be ~2:1 to 5:1. However, this experiment does indeed demonstrate more complex functionalities than have been previously demonstrated using quantum well logic devices.

III. Differential Logic Family

The second class of circuits, which has quantum well diode configurations similar to transistors in CMOS,[14] represents the logic state by the relative intensities in a set of two beams as was the case in the S-SEED logic gate.[8] These differential logic gates also avoid critical biasing, have time-sequential gain, good input/output isolation and signal retiming. In addition, these gates do not need a reference signal to be generated.

A general logic gate is shown in Fig. 8. As before, in many cases the same quantum well PIN diodes can be used for the detection and modulation processes, but for simplicity, the circuits that we present here have

Table II. Truth table for $E = AB + CD$, calculated currents assume a responsivity of 1 A/W

D	C	B	A	E	i_A	i_B	i_{AB}	i_C	i_D	i_{CD}	i_{AB+CD}
0	0	0	0	0	P_0	P_0	P_0	P_0	P_0	P_0	$2P_0$
0	0	0	1	0	P_1	P_0	P_0	P_0	P_0	P_0	$2P_0$
0	0	1	0	0	P_0	P_1	P_0	P_0	P_0	P_0	$2P_0$
0	0	1	1	1	P_1	P_1	P_1	P_0	P_0	P_0	(P_0+P_1)
0	1	0	0	0	P_0	P_0	P_0	P_1	P_0	P_0	$2P_0$
0	1	0	1	0	P_1	P_0	P_0	P_1	P_0	P_0	$2P_0$
0	1	1	0	0	P_0	P_1	P_0	P_1	P_0	P_0	$2P_0$
0	1	1	1	1	P_1	P_1	P_1	P_1	P_0	P_0	(P_0+P_1)
1	0	0	0	0	P_0	P_0	P_0	P_0	P_1	P_0	$2P_0$
1	0	0	1	0	P_1	P_0	P_0	P_0	P_1	P_0	$2P_0$
1	0	1	0	0	P_0	P_1	P_0	P_0	P_1	P_0	$2P_0$
1	0	1	1	1	P_1	P_1	P_1	P_0	P_1	P_0	(P_0+P_1)
1	1	0	0	1	P_0	P_0	P_0	P_1	P_1	P_1	(P_0+P_1)
1	1	0	1	1	P_1	P_0	P_0	P_1	P_1	P_1	(P_0+P_1)
1	1	1	0	1	P_0	P_1	P_0	P_1	P_1	P_1	(P_0+P_1)
1	1	1	1	1	P_1	P_1	P_1	P_1	P_1	P_1	$2P_1$

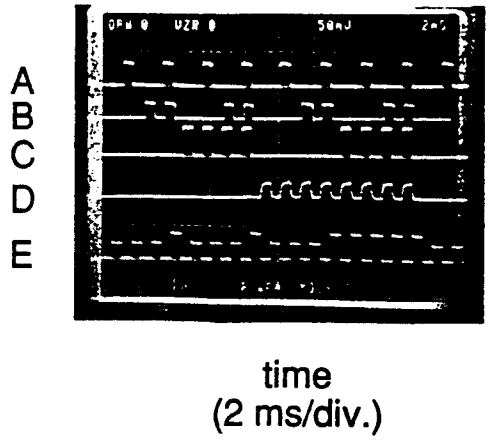

Fig. 7. Experimental results of the logic gate implementing $E = AB + CD$. The circuit consisted of a 1 × 2 S-SEED array electrically connected to a the center node of a single S-SEED. The truth table is given in Table II.

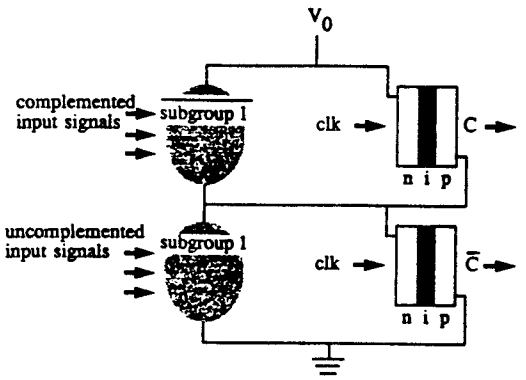

Fig. 8. Differential logic gate. Output C is the noninverting (i.e., ORs and ANDs) uncomplemented output and output $\bar{C}$ is the complemented output. Diodes in subgroup 1 are electrically interconnected in a manner known as the conduction complement to the diodes in $\overline{\text{subgroup 1}}$.

separate diodes on which the input signals are incident and on which the clock beams that generate the output beams are incident. Also, the diodes that do not generate output beams do not need quantum wells, although improved switching may result with quantum wells as discussed above. Each logical input uses two complementary beams to represent the logic state. If the power of the uncomplemented beam is greater than the complemented beam, this input will be defined as a logic one; a logic zero is the reverse case. Two sets of PIN diodes accept the incident input signals, subgroup 1, with uncomplemented input signals, and $\overline{\text{subgroup 1}}$, with complemented input signals. Instead of connecting subgroup 1 in series with a diode with an incident reference beam, subgroup 1 and $\overline{\text{subgroup 1}}$ are now connected in series. The diodes in $\overline{\text{subgroup 1}}$ are electrically interconnected in a manner known as the conduction complement[14] of the connections of the diodes in subgroup 1. For example, if subgroup 1 consists of serially connected diodes, $\overline{\text{subgroup 1}}$ consists of parallel connected diodes. The voltage at the interconnecting node between subgroup

1 and subgroup 1 is connected to the center node of an output S-SEED and, thus, determines the output state of the device. For noninverting functions (i.e., ANDs and ORs), output C is the uncomplemented output, and output $\bar{C}$ is the complemented output. For inverting functions (i.e., NANDs and NORs), the outputs are reversed. That is, the output labeled C becomes the complemented output, the output labeled $\bar{C}$ becomes the uncomplemented output. In either case, we define the output state to be a logic one when the power of the uncomplemented output beam is greater than that of the complemented output beam.

In operation, first the signal beams are applied to the respective diodes. The voltage that will be present on the node between the two sets of signal diodes will be a function of the currents generated by these diodes. The voltage across subgroup 1 in Fig. 8 must be essentially zero, if the logic function is not satisfied, for the output to be a logic zero (output $\bar{C}$ greater than C). This will occur if the photocurrent generated by subgroup 1 is initially less than that generated by subgroup 1. Conversely, the voltage across subgroup 1 must be essentially equal to the supply voltage, if the logic function is satisfied, for the output to be a logic one (output C greater than $\bar{C}$). In this case, the photocurrent generated by subgroup 1 must be initially greater than that generated by subgroup 1. These two cases will be automatically satisfied provided that the input signals have sufficient contrast ratios. We can also add attenuators in the path of certain input signals to operate the circuit optimally for low contrast ratios. If we are using quantum well PIN diodes for the detector diodes, there is a range of input power levels where bistability exists and this will place a lower limit on the contrast ratio of the input signals. However, if we again ramp the supply voltage up from zero during the application of the input signals, effectively removing any bistable characteristics, the circuits can be made to work with any input contrast greater than one. As before, the node between the two groups of input diodes is electrically connected to the node between the two diodes of the output S-SEED. Therefore, once the voltage at this point has been determined (i.e., after the switching time of the circuit), we can remove the signal beams and apply the clock beams of higher power achieving time-sequential gain.

The circuit shown in Fig. 9(a) implements a differential AND gate. The two complementary input signals are represented by light beams A and $\bar{A}$ and light beams B and $\bar{B}$. A pair of clock beams, incident on the output S-SEED, generates output beams C and $\bar{C}$. The two uncomplemented signals, A and B, are incident on two serially connected diodes, and the complemented signals, $\bar{A}$ and $\bar{B}$, are incident on two parallel connected diodes. If either or both of beams A and B are low, one of beams $\bar{A}$ and $\bar{B}$ must be high, because the input signals are complementary. Therefore, the current generated by the serially connected diodes will be initially less than that generated by the parallel connected diodes (for any contrast), so the voltage at

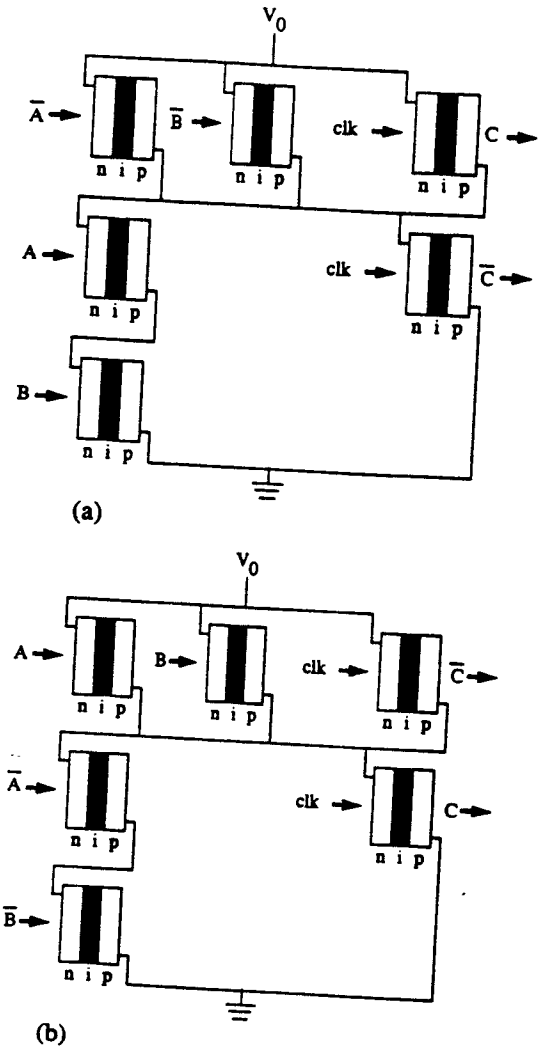

Fig. 9. Differential logic gates implementing the four basic logic functions: (a) AND/NAND gate: $C = AB$, $\bar{C} = \overline{AB}$; (b) OR/NOR gate: $C = A + B$, $\bar{C} = \overline{A + B}$. For the gate to operate at contrast ratios less than 2:1, inputs on parallel connected diodes must be attenuated by 50%.

the center node of the output S-SEED will be essentially equal to the supply voltage. Thus, when the clock beams are applied, the output will be a logic zero because output beam C will be low and output beam $\bar{C}$ will be high. If input beams A and B are both high, input beams $\bar{A}$ and $\bar{B}$ must both be low because they are complementary to input beams A and B. Assuming that the sum of optical powers of the two low beams is less than that of one high beam, the current generated by serially connected diodes will be initially greater than that generated by the parallel connected diodes. In this case, the voltage at the center node of the output S-SEED will essentially be equal to zero. When the clock beams are applied, output C will be high and output $\bar{C}$ will be low and thus the output state is a logic one. Therefore, this logic gate performs an AND function. Conversely, if we define the output state as being a logic one when the power in output beam $\bar{C}$ is greater than that of beam C, the circuit performs a NAND function.

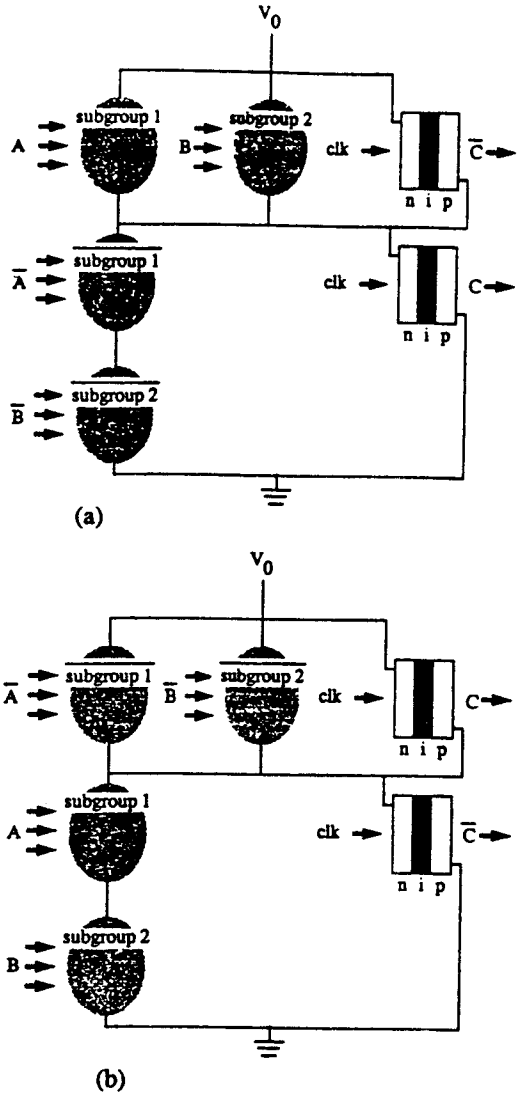

Fig. 10. Combinations of subfunctions implemented with differential logic gates. (a) (C = subfunction 1 + subfunction 2, $\bar{C}$ = $\overline{\text{subfunction 1 + subfunction 2}}$); (b) ($C$ = subfunction 1 · subfunction 2, $\bar{C}$ = $\overline{\text{subfunction 1 · subfunction 2}}$).

Fig. 9(b) shows an OR/NOR gate. This circuit is identical to the AND/NAND circuit with the inputs and outputs reversed and can be analyzed using similar arguments. If we define a logic one as being when the power of output beam C is greater than that of output beam $\bar{C}$, this circuit performs an OR function. Similarly, if the output is a logic one when the power of output beam $\bar{C}$ is greater than that of output beam C, the circuit performs a NOR function.

An N input logic gate can be realized in a similar manner. Instead of two serially connected diodes, there are now N (uncomplemented) input signals incident on N serially connected diodes, and N complemented signals incident on N parallel connected diodes. As an example, an N input AND gate will have the desired output a logic one if all inputs are logic ones and a logic zero if at least one input is a logic zero. These two conditions are satisfied if $P_{\text{LOGIC1}} > NP_{\text{LOGIC0}}$ and $P_{\text{LOGIC0}} < P_{\text{LOGIC1}} + (N-1)P_{\text{LOGIC0}}$.

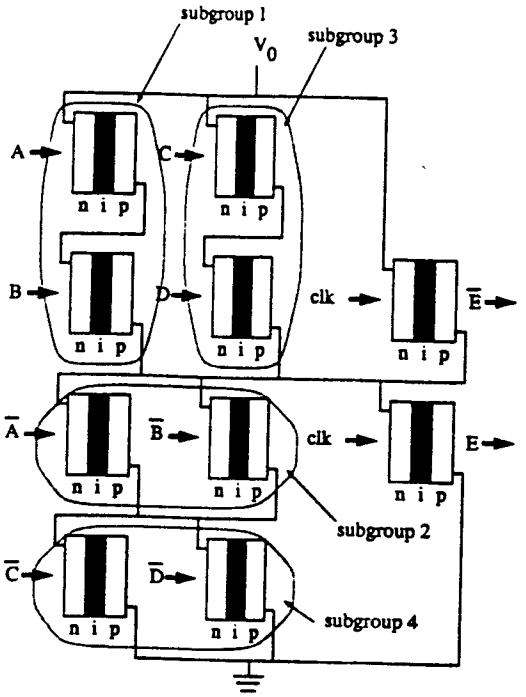

Fig. 11. Differential logic gate implementing $E = AB + CD$.

The first condition is only satisfied for input contrast ratios greater than N:1 and the second condition is always satisfied. An attenuator added in the path of the input beams incident on the parallel connected diodes that transmits $1/N$ of the incident power enables this logic gate to be used for any contrast ratio (assuming that the bistable characteristics are removed).

The method of realizing arbitrary functions is similar to the single ended gates as illustrated in Fig. 10. For the uncomplemented signals, the OR [Fig. 10(a)] and AND [Fig. 10(b)] of two subfunctions is achieved by electrically connecting their respective subgroups of PIN diodes in parallel and series, respectively, as before. However, the subgroups of diodes with incident complemented signals are connected in series and parallel for OR and AND functions, respectively. The diodes with the uncomplemented inputs are connected in series with the diodes with the complemented inputs. The center node between these two groups of diodes is connected to the center node of the output S-SEED and the voltage on this node determines the relative outputs of the S-SEED.

Again, as an example, let us consider a function given by $E = AB + CD$. The differential logic gate shown in Fig. 11 implements this function. Subgroup 1 consists of two diodes with incident input beams A and B connected electrically in series. Subgroup 2 consists of two diodes with incident input beams $\bar{A}$ and $\bar{B}$ connected electrically in parallel. As we have seen above, subgroups 1 and 2 implement an AND function of A and B. Similarly, subgroup 3 consists of two diodes with incident input beams C and D connected electrically in series, and subgroup 4 consists of two diodes with incident input beams $\bar{C}$ and $\bar{D}$ connected electrically in parallel. Subgroups 3 and 4 implement

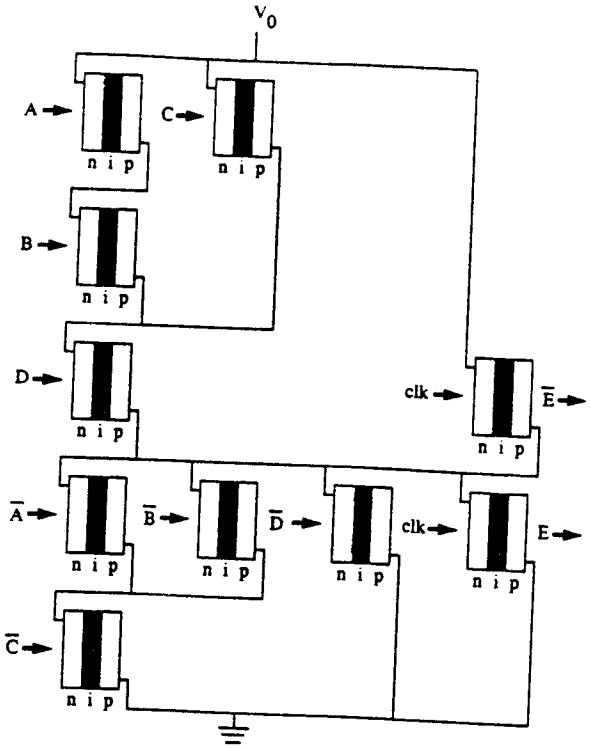

Fig. 12. Differential logic gate implementing $E = (AB + C)D$. For the gate to operate at contrast ratios less than 3:1, inputs $\bar{A}$ and $\bar{B}$ should be attenuated by 75%, inputs A, B, C, $\bar{C}$, and $\bar{D}$ should be attenuated by 50%, and input D is unattenuated.

the AND function of C and D. To implement the OR of AB and CD, connect subgroups 1 and 3 in parallel and subgroups 2 and 4 in series.

A general PLA can be made as follows. Referring to Fig. 8, subgroup 1 consists of p parallel connected groups of s_p serially connected diodes. Subgroup 1 consists of p serially connected groups of s_p parallel connected diodes. In this circuit no attenuators are needed to ensure operation of the gate at any contrast ratio greater than one (again, assuming no bistability while the input signals are applied), provided $s_p = p$.

We can also consider truly arbitrary functions such as the one described in Fig. 6 and given by $E = (AB + C)D$. The circuit for implementing this function in differential logic is shown in Fig. 12. The contrast ratio of the input signals must be greater than 3:1 for the circuit to operate properly, because a logic one for input D must generate more current than the sum of the currents generated by logic zeros for inputs $\bar{A}$, $\bar{B}$, and $\bar{D}$. To operate at any contrast ratio greater than one, signals $\bar{A}$ and $\bar{B}$ must be attenuated by 75%; signals A, B, C, $\bar{C}$, and $\bar{D}$ need to be attenuated by 50%, and signal D is unattenuated.

To show the functionality of these gates, we demonstrated operation of the logic gate in Fig. 11 ($E = AB + CD$) using seven S-SEEDs on four different arrays, as illustrated in Fig. 13. Nine semiconductor diode lasers provided the four uncomplemented signal beams, four complemented signal beams, and the set of two clock beams. As before, the lasers were driven by a digital word generator. In fact, because we did not

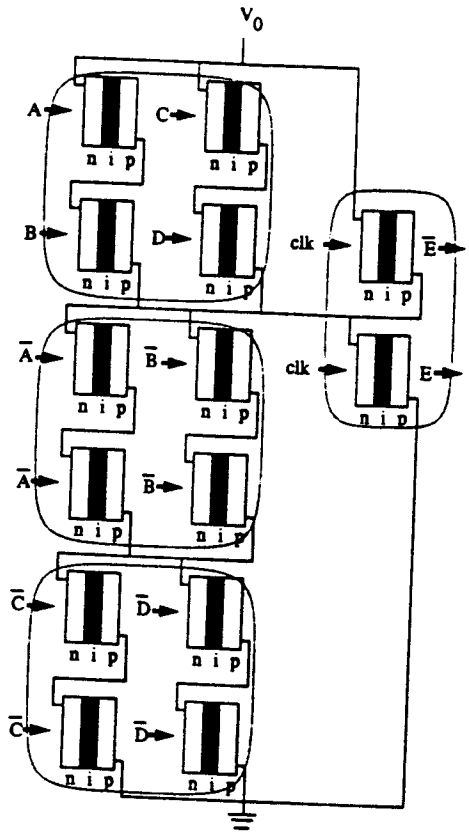

Fig. 13. Circuit used to obtain the experimental results of the differential logic gate implementing $E = AB + CD$. Single diodes in Fig. 11 with incident complemented input signals were replaced by two diodes because we did not have any single diodes. (Performance of this circuit should be identical to that shown in Fig. 11.) Circles outline the four discrete arrays of S-SEEDs used.

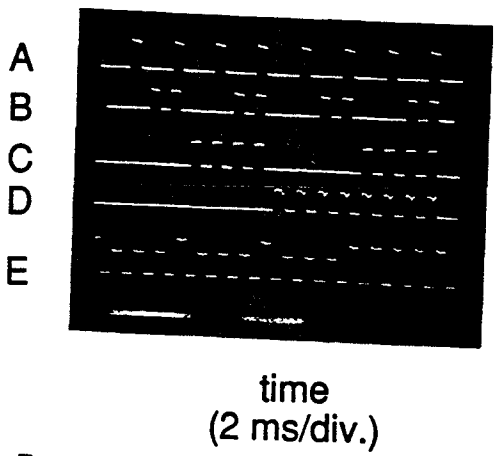

Fig. 14. Experimental results of the logic gate implementing $E = AB + CD$, shown in Fig. 13. The truth table is given in Table II.

have sufficient single quantum well diodes available, we utilized series pairs (S-SEEDs) in which both diodes were illuminated for some parts of the circuit. The four uncomplemented input signals and noninverting output signal are shown in Fig. 14. Since the S-SEEDs were connected with long coaxial cables, no attempt was made to measure the optical switching

energy and compare that with theoretical switching energy. However, we have proven the correct functionality for this circuit as can be seen by comparing the noninverting output to the truth table in Table II.

IV. Conclusion

We have presented two novel classes of self-electrooptic effect devices or circuits consisting of electrically connected quantum well PIN diodes that are capable of performing any optical logic function. One class of circuits, which has PIN diode configurations similar to transistor configurations in NMOS, compares the input signals to locally generated reference beams. By using reference beams derived from the same laser that generates the signal inputs, we have a logic family that is insensitive to optical power supply fluctuations. The other class of circuits, which has PIN diode configurations similar to transistor configurations in CMOS, routes signals as differential pairs, eliminating the need to compare to a reference signal. For both logic families, we have demonstrated the function $E = AB + CD$, which to our knowledge, is the most complex logic function demonstrated to date with quantum well optoelectronic devices. Since both classes of circuits have time-sequential gain, have input/output isolation, perform retiming of the signals, and lack critical biasing, they retain good physical functionality in that they are easy to use. This, coupled with the fact that they can implement arbitrary logic functions, makes them potentially very useful for future optical signal processing systems.

We would like to acknowledge the assistance of S. J. Hinterlong for supplying the laser diodes and D. B. Buchholz, R. L. Morrison, and S. L. Walker for supplying the 1 × 2 binary phase gratings that were used in the experiments. Additionally, we would like to thank R. F. Kopf and C. W. Tu for growing the material and M. W. Focht for assisting in the fabrication of some of the devices used in the experiments.

References

1. See, e.g., H. M. Gibbs, *Optical Bistability: Controlling Light with Light* (Academic, New York, 1985); J. L. Jewell, A. Sherer, S. L. McCall, A. C. Gossard, and J. H. English "GaAs–AlAs Monolithic Microresonator Arrays," Appl. Phys. Lett. 51, 94–96 (1987).
2. D. A. B. Miller *et al.*, "The Quantum Well Self-Electro-Optic Effect Device: Optoelectronic Bistability and Oscillation, and Self-Linearized Modulation," IEEE J. Quantum Electron. QE-21, 1462–1476 (1985).
3. See, e.g., D. A. B. Miller, J. S. Weiner, and D. S. Chemla, "Electric Field Dependence of Linear Optical Properties in Quantum Well Structures: Waveguide Electro-Absorption and Sum Rules," IEEE J. Quantum Electron. QE-22, 1816–1830 (1986).
4. D. A. B. Miller *et al.*, "Novel Hybrid Optically Bistable Switch: The Quantum Well Self-Electro-Optic Effect Device," Appl. Phys. Lett. 45, 13–15 (1984).
5. D. A. B. Miller, J. E. Henry, A. C. Gossard, and J. H. English, "Integrated Quantum Well Self Electro-Optic Effect Device: 2 × 2 Array of Optically Bistable Switches," Appl. Phys. Lett. 49, 821–823 (1986).
6. G. L. Livescu, D. A. B. Miller, J. E. Henry, A. C. Gossard, and J. H. English, "Spatial Light Modulator and Optical Dynamic Memory Using a 6 × 6 Array of Symmetric Self-Electro-Optic Effect Devices," Optics Lett. 13, 297–299 (1988).
7. A. L. Lentine, H. S. Hinton, D. A. B. Miller, J. E. Henry, J. E. Cunningham, and L. M. F. Chirovsky, "Symmetric Self-Electro-Optic Effect Device: Optical Set-Reset Latch," Appl. Phys. Lett. 52, 1419–1421 (1988); "Symmetrtic Self-Electro-Optic Effect Device: Optical Set-Reset Latch, Differential Logic Gate and Differential Modulator/Detector," IEEE J. Quantum Electron. QE-25, 1928–1936 (1989).
8. A. L. Lentine, D. A. B. Miller, J. E. Henry, and J. E. Cunningham, "Photonic Ring Counter and Differential Logic Gate Using the Symmetric Self-ElectroOptic Effect Device," in *Technical Digest, Conference on Lasers and Electro-Optics* (Optical Society of America, Washington DC 1988), paper TuE4.
9. L. M. F. Chirovsky, L. A. D'Asaro, C. W. Tu, A. L. Lentine, G. D. Boyd, and D. A. B. Miller, "Batch Fabricated Symmetric Self-Electrooptic Effect Devices," in *Technical Digest, Topical Meeting on Photonic Switching*, (Optical Society of America, Washington DC 1989), paper ThD4.
10. A. L. Lentine, L. M. F. Chirovsky, L. A. D'Asaro, C. W. Tu, and D. A. B. Miller, "Performance Scaling and Subnanosecond Switching of Symmetric Self-Electrooptic Effect Devices," in *Technical Digest, Conference on Lasers and Electro-Optics* (Optical Society of America, Washington DC., 1989), paper WO3.
11. A. L. Lentine, D. A. B. Miller, J. E. Henry, J. E. Cunningham, and L. M. F. Chirovsky, "Multistate Self-Electrooptic Effect Devices," in *Technical Digest, OSA Annual Meeting* (Optical Society of America, Washington DC, 1988); IEEE J. Quantum Electron. QE-25, 1921–1927 (1989).
12. See, e.g., H. S. Hinton, "Architectural Considerations for Photonic Switching Networks," IEEE J. Select. Areas Commun. SAC-6, 1209–1226 (1988).
13. D. A. B. Miller, "Nonlinear and Bistable Optical Device," U.S. Patent 4,546,244, (1985), 4,716,449 (1987).
14. J. Allen, *Introduction to VLSI Design: NMOS, CMOS* (Addison-Wesley, Reading, MA 1980).
15. P. Wheatley *et al.*, "Novel Nonresonant Optoelectronic Logic Device," Electron. Lett. 23, 92 (1987).
16. N. C. Craft and M. E. Prise, "Optical Systems Tolerances for Symmetric Self-Electrooptic Effect Devices in Optical Computers," in *Topical Meeting on Optical Computing*, (Optical Society of America, Washington, DC, 1989), paper Tul29.
17. M. E. Prise, M. M. Downs, F. B. McCormick, S. J. Walker, and N. Streibl, "Design of An Optical Digital Computer," in *Optical Bistability IV*, W. J. Firth *et al.*, Eds. (Les Editions de Physique, Paris, 1988).