If parity of β is even, $Q(Z)$ has two distinct roots specified by eqns. 6 and 8, and in the case of odd parity, there are no roots. Parity of the constant β is given by eqn. 9.

$$\text{parity } (\beta) = \sum_{i=0}^{m-1} b_i \tag{9}$$

Now the hardware structure can be designed based on eqns. 6, 8 and 9 which has a propagation delay of only $[m/2]$ XOR gates.

As an illustrative example let us consider GF(2^8), which can be generated using 16 different irreducible polynomials in normal basis representation.[5] The hardware solution for the translated quadratic equation, $Z^2 \oplus Z \oplus \beta = 0$ in GF(2^8) is given in Fig. 1. This structure is independent of the generating polynomials and it is the same for all of the 16 polynomials which can represent a normal basis in GF(2^8).

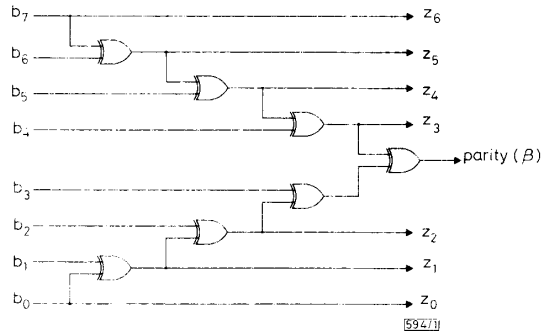

Fig. 1 *Hardware solution for* $Z^2 \oplus Z \oplus \beta = 0$ *in GF*(2^8)

This structure needs seven XOR gates to find $Z_1 = [0, z_6, z_5, z_4, z_3, z_2, z_1, z_0]$ and parity $(\beta) = \sum_{i=0}^{7} b_i$. If parity $(\beta) = 0$, Z_1 is one of the solutions and the other solution, $Z_2 = [1, \bar{z}_6, \bar{z}_5, \bar{z}_4, \bar{z}_3, \bar{z}_2, \bar{z}_1, \bar{z}_0]$ can be found using seven INV gates. The propagation delay of the structure is equivalent to the delay of four XOR gates.

This hardware structure, which is based on eqns. 6, 8 and 9 has the following advantages compared to structures in non-normal bases.[2] Note that all these advantages are due to the squaring property of the normal basis representation which was used to form system of equations given in eqn. 4.

The main advantage of this structure is independence with respect to the generating polynomial of the field. In other words, the existence of the solutions and solutions themselves depend only on the size of each element (m), not on the generating polynomial of the field, as long as the generating polynomial represents a normal basis. However, in non-normal basis representations, the solution of the translated quadratic equation depends on the generating polynomial of the field[2] even with a fixed value for the element size.

This structure is simple, regular and expandable. The condition for existence of the solutions is just a parity check operation (eqn. 9), and the solutions can be easily found by a simple and regular structure given by eqns. 6 and 8. If the size of each element is m bits, there will be a need for $m - 1$ XOR gates. To find the second root, $m - 1$ INV gates are also needed. This structure can be expanded to an $m + 1$ element size structure very easily just by adding one more XOR and one INV gate. Note that in non-normal representations, the structure of the system is not as simple as the case of normal basis and it cannot be expanded to the $m + 1$ element size structure.[2]

Conclusion and application: In this letter a new direct solution for a quadratic equation defined in a Galois field, based on a normal basis, was introduced. It was shown that the proposed solution was independent of the generating polynomial of the field, as long as the generating polynomial represented a normal basis. Then a new, simple, regular and expandable hardware structure was introduced to find the roots of $Z^2 \oplus Z \oplus \beta = 0$. The advantages of using a normal basis representation as compared to non-normal ones were discussed. It was shown that all the advantages are due to the squaring property of this representation.

The error locator polynomial for double error correcting Reed–Solomon (RS) decoders is a quadratic equation defined in Galois fields. Therefore the proposed approach and the hardware structure can be used in decoding double error correcting RS codes. This representation also decreases the complexity of the multiplication and inversion circuitry needed for decoding. In normal basis representation a Massey–Omura multiplier and the inversion circuit based on this multiplier[4] can be used.

Y. R. SHAYAN
THO LE-NGOC

Department of Electrical and Computer Engineering
Concordia University
1455 de Maisonneuve Blvd. West
Montreal, Quebec, Canada H3G 1M8

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References

1 POLKINGHORN, F.: 'Decoding of double and triple error correcting Bose–Ch'audhuri codes', *IEEE Trans.*, 1966, **IT-12**, pp. 480–481
2 HEISE, N. N., and KRZYSTAN, T. J.: 'Direct hardware solution to the quadratic equation $y^2 + y + c = 0$ in GF(2^m)', *IBM Tech. Disclosure Bull.*, 1985, **27**, pp. 4767–4771
3 MACWILLIAMS, F. J., and SLOANE, N. J. A.: 'The theory of error-correcting codes' (North-Holland, New York, 1977)
4 WANG, C. C., TRUONG, T. K., SHAO, H. M., DEUTSCH, L. J., OMURA, J. K., and REED, I. S.: 'VLSI architectures for computing multiplications and inverses in GF(2^m)', *IEEE Trans.*, 1985, **C-34**, pp. 709–717
5 PETERSON, W. W., and WELDON, E. J., JUN.: 'Error-correcting codes' (MIT Press, Cambridge, MA, 1972)

ALL-OPTICAL REGENERATOR

Indexing terms: Optical communications, Optical processing, Lasers and laser applications, Optical transmission

An all-optical regenerator has been demonstrated using two self-electro-optic effect devices (SEED) and a local pump laser. The regenerator's optical signal processing included clock recovery, data retiming and signal amplification. A 2dB optical gain was attained at a 5kbit/s data rate.

Introduction: Long-distance optical transmission systems usually are comprised of several fibre spans, each terminated with an optoelectronic regenerative repeater. These regenerative repeaters restore the weak and distorted incoming optical signals back to a high level in the original state for transmission through the following span. The signal regeneration, including clock recovery and pulse reshaping, is done in the electrical domain after signal detection with a photodetector, and only in the final stage is the signal converted back to light by electrically modulating a semiconductor laser.

An alternative to the optoelectronic regenerator is one where optical signals exist at all stages of signal processing. We report in this letter, the first such 'all-optical' regenerator which, by virtue of its optical continuity, has simplified signal processing, and has the potential for very high-speed operation. This regenerator consisted of two discrete self-electro-optic-effect devices (SEEDs)[1] within an electrically and optically powered circuit. One SEED, configured to self-pulsate, produced optical clock pulses synchronised to the incoming signal, while the other SEED acted as the decision element whose output was the regnerated signal. These two SEEDs and a pump laser are the only active components needed in the regenerator to accomplish signal detection, clock recovery, data retiming, and optical retransmission.

Experiment: Fig. 1 shows the experimental set-up for the all-optical regenerator. A 10mW, 0·85 μm AlGaAs semiconductor laser provided the pump beam to power the regenerator. A

similar laser produced the test signal. The SEED consisted of 50–70 μm-long waveguide multiple-quantum-well modulators whose six GaAs quantum wells, each 105 Å thick, were in the

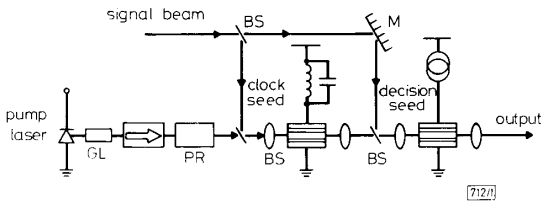

Fig. 1 *All-optical regenerator*
BS = beamsplitter; GL = GRIN lens; PR = polarisation rotator

centre of a 0·59 μm-thick undoped region of a back-biased *pin* diode.[2] Optical absorption within such SEEDs exhibits strong electric-field dependence at wavelengths close to the exciton resonance peak.[3] Under appropriate feedback conditions with passive electrical networks connected to the SEED, several active optical components can be constructed, including the clock oscillator and threshold decision devices used here.[1]

The clock recovery SEED was electrically biased through a parallel *LC* circuit and had the pump laser beam focused into its waveguide region with a microscope objective lens. The resultant negative-resistance oscillator functions to modulate the CW pump beam, producing a continuous train of optical pulses. A fraction of the input signal beam is combined with the pump beam through a beamsplitter to injection-lock this oscillator to the signal data rate. Linearised analysis of the lock-in oscillator, which is the same as that for an electrical oscillator,[4] gives a frequency lock-in range of $\Delta f = \pi\,\delta I f_0^2 L/V$ about the centre frequency $f_0 = 1/2\pi\sqrt{(LC)}$ where δI and V are the peak/peak values of the injection signal photocurrent and oscillator voltage respectively. Fig. 2 shows the output

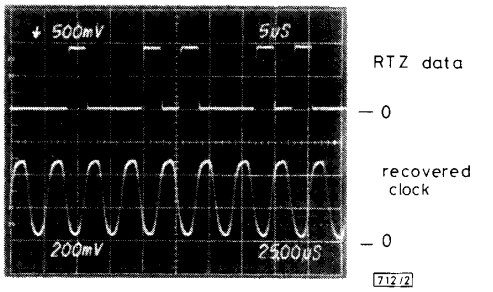

Fig. 2 *Injection-locking of clock-recovery SEED output to RTZ signal*
Upper trace = 173 kbit/s RTZ datastream; lower trace = recovered clock signal

from one oscillator synchronised to a 173 kbit/s pseudorandom data stream upon injecting 6 μW of signal power. Within the lock-in range $|\Delta f| = 700$ Hz, the relative phase of the clock pulses to the lock-in signal varied between $\pm 90°$ with signal frequency about f_0. This phase variation, typical of injection-locked oscillators and first-order phase locked loops, did not impair regeneration at fixed data rates and input power levels.

The second SEED, being the decision element controlled by the recovered optical clock and the input optical signal, produced the regenerated optical signal. Its constant current bias came from a low-capacitance photodiode illuminated by an LED light source. Furthermore, the upper and lower compliance voltages of the current source were separately adjustable through diode voltage clamps. The SEED operated either as an AND gate or a bistable switch, depending upon the values of these compliance voltages, as indicated in Fig. 3. This Figure shows the SEED optical output and photocurrent against applied voltage, for constant incident light power. When the SEED is used as an AND gate, both clock and data must be high in order to raise the SEED photocurrent, I_{SEED}, to where it equals the current source value, I_{SOURCE}, with 0 V across the SEED. This voltage coincides with the SEEDs high transmission state. If either clock or data is low, then $I_{SEED} = I_{SOURCE}$ at the voltage where the SEED is strongly absorbing, causing a low transmission state. In this manner, the SEED transmission of the input signal is gated by the clock pulses.

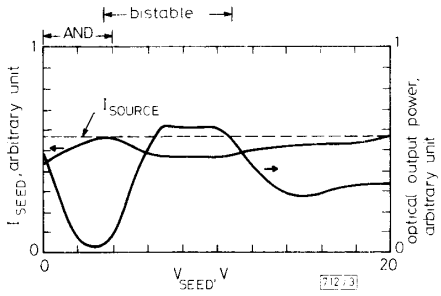

Fig. 3 *SEED transmission and photocurrent curves for constant input optical power with indicated compliance voltage ranges for AND and bistable switching*

Bistable-switching circuits, such as D-flip-flops, rather than AND gates, are commonly used as decision circuits in electronic regenerators. These retime the data, removing phase jitter in the data stream that otherwise will progressively worsen through multiple regeneration in long-distance transmission. The bistable SEED switch, like the D-flip-flop, can also retime data during regeneration. The only change in SEED operation to obtain the bistable switching, is an adjustment of the current source compliance voltages as indicated in Fig. 3. In addition to retiming, data are also inverted when passed through the bistable SEED, providing additional design flexibility.

Results: With the cascaded circuit of the clock recovery SEED followed by the decision SEED, regeneration was done both with AND gate and bistable switching. The long switching time of the decision SEED limited the regenerator's maximum signalling rate: a 5 kbit/s rate was chosen so that the signal characteristics could be readily observed. The speed limitation resulted from having to discharge the decision circuit's parasitic capacitance, C_P, with small photocurrents so that the switching time, $C_P V/I_{SEED}$, was typically 10 μs.

Fig. 4 shows input and output optical waveforms of a '010' segment of return-to-zero data for both AND gate and

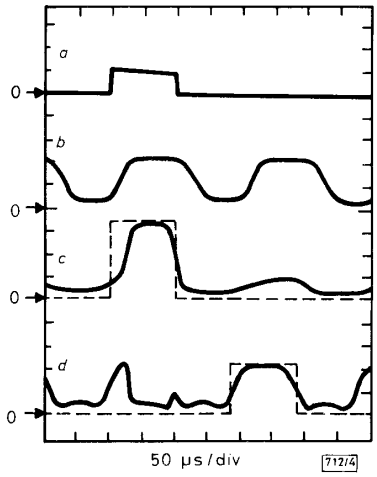

Fig. 4 *Optical signals in all-optical regenerator*
a Input '010' RTZ data
b Recovered optical clock
c Output from AND gate decision SEED
d Output from bistable decision SEED
Broken curves are ideal regenerated waveforms

bistable switching. These results were obtained with the clock-recovery SEED average photocurrent equal to 1·5 mA, of which 2 μA was the lock-in signal photocurrent. The optical clock and signal beam in the decision SEED produced average photocurrents of 13·1 μA and 1·7 μA respectively.

Stable injection-locking and well defined switching were obtained with these photocurrent levels.

Switching with an AND gate was attained with the current source set to 15 μA and its voltage limited to between 0 and 4 V. Good contrast, 5·5 dB, between the '0' and '1' levels was obtained with no significant impairment in the reshaped output signal. Next, the decision SEED was operated bistably by setting the current-source voltage limits to 3·5 and 11 V. The SEED oscillator bias was adjusted slightly to obtain a more symmetric waveform. The inverted output signal had good level contrast, but a 30 μs wide triangular pulse appeared as an artefact in the low output state. This pulse resulted from the slow risetime of the clock pulse, causing a delay before the SEED switched to the low state. This feature could be removed by speeding up the clock transitions with a second bistable SEED positioned after the clock oscillator. Even with this extraneous pulse, the energy ratio between the regenerated 1s and 0s was better than 2 : 1.

Optical gain through the bistable regenerator was achieved with a signal power of 0·87 μW injected into both the clock recovery and decision SEEDs. The output optical power of the decision SEED was 3·28 μW, which after correcting for the output extinction ratio, corresponded to a 2 dB gain in the peak/peak signal power through the regenerator. High absorption losses through the SEEDs ($\approx$11 dB each) and optical coupling losses between stages ($\approx$8 dB total) caused the low observed gain. However, the decision circuit easily distinguished between 0s and 1s when the injected clock power was 15 dB greater than the signal power. Without optical amplifiers, this switching gain, minus the loss through the decision SEED, is the maximum expected gain in this type of regenerator.

Summary: An all-optical regenerator based on AlGaAs–GaAs multiple-quantum-well SEEDs has been demonstrated. We believe that this is the first all-optical regenerator capable of signal detection, clock recovery and data retiming. Regeneration of 5 kbit/s RTZ signals with 2 dB gain was demonstrated, although the inherent speed limitations in the proposed configuration suggest that the circuit could operate at much higher rates.[5] The regenerator's simplicity is suited to monolithic integration, which together with higher optical pump powers, might permit such high-speed operation in future optical circuits.

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C. R. GILES
T. LI
T. H. WOOD
C. A. BURRUS

AT&T Bell Laboratories
Crawford Hill Laboratory
Holmdel, NJ 07733, USA

D. A. B. MILLER

AT&T Bell Laboratories
Holmdel, NJ 07733, USA

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References

1 MILLER, D. A. B., CHEMLA, D. S., DAMEN, T. C., WOOD, T. H., BURRUS, C. A., GOSSARD, A. C., and WIEGMANN, W.: 'The quantum well self-electro-optic effect device: optoelectronic bistability and oscillation, and self-linearized modulation', *IEEE J. Quantum Electron.*, 1985, **QE-21**, pp. 1462–1476

2 WOOD, T. H., BURRUS, C. A., TUCKER, R. S., WEINER, J. S., MILLER, D. A. B., CHEMLA, D. S., DAMEN, T. C., GOSSARD, A. C., and WIEGMANN, W.: '100 ps waveguide multiple quantum well (MQW) optical modulator with 10 : 1 on/off ratio', *Electron. Lett.*, 1985, **21**, pp. 693–694

3 MILLER, D. A. B., CHEMLA, D. S., DAMEN, T. C., GOSSARD, A. C., WIEGMANN, W., WOOD, T. H., and BURRUS, C. A.: 'Bandedge electroabsorption in quantum well structures: the quantum confined stark effect', *Phys. Rev. Lett.*, 1984, **53**, pp. 2173–2177

4 KUROKAWA, K.: 'Injection locking of microwave solid-state oscillators', *Proc. IEEE*, 1973, **61**, pp. 1386–1410

5 SCHMITT-RINK, S., CHEMLA, D. S., and MILLER, D. A. B.: 'Theory of transient excitonic optical nonlinearities in semiconductor quantum-well structures', *Phys. Rev. B.*, 1985, **32**, pp. 6601–6609

5 GHz JOSEPHSON A/D CONVERTOR

Indexing terms: Analogue/digital conversion, Convertors, Josephson junctions, Superconducting devices

A four-bit A/D convertor using Nb/AlO_x/Nb Josephson junctions was fabricated. The circuit was designed to preserve the matching of characteristic impedances at all nodes. Four-bit A/D conversion was confirmed at a low frequency. The A/D convertor correctly operated at up to 5 GHz for two-bit conversion.

Introduction: Several types of A/D convertor using Josephson junctions have been proposed.[1–5] Josephson A/D convertors are generally characterised by a high-speed conversion rate and a small number of comparators. Only N comparators are necessary to compose a flash-type N-bit A/D convertor.

The Josephson A/D convertor proposed by Hamilton *et al.*[2] has the simplest construction, i.e., one comparator consists of one superconducting quantum interference device (SQUID). We designed and fabricated this type of four-bit A/D convertor.

Design: Fig. 1 shows the equivalent circuit of the SQUID designed as a comparator. The designed critical current density is 3000 A/cm^2.

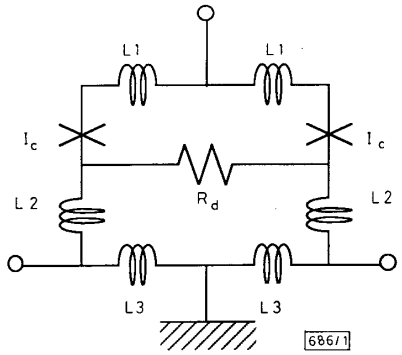

Fig. 1 *Equivalent circuit of SQUID designed as comparator*
I_c = 0·21 mA, $L1$ = 0·25 pH, $L2$ = 0·8 pH, $L3$ = 1·4 pH, R_d = 2·4 Ω

Fig. 2 shows the equivalent circuit of the designed four-bit A/D convertor. In designing the circuit, it is important to match the characteristic impedance for superconducting wiring at every node. This is vital to operating the circuit at a frequency over 1 GHz. In measurements with a high clock frequency, 50 Ω coaxial cables connect measuring instruments with an A/D convertor chip immersed in liquid helium. Therefore, it is desirable to design the impedance of the superconducting strip lines in the chip to be 50 Ω. This results in a 0·5 μm-wide strip line. However, 0·5 μm-wide Nb lines are hard to fabricate, so we designed the line to be 4 Ω for the power supply. Line impedance at I/O terminals was converted

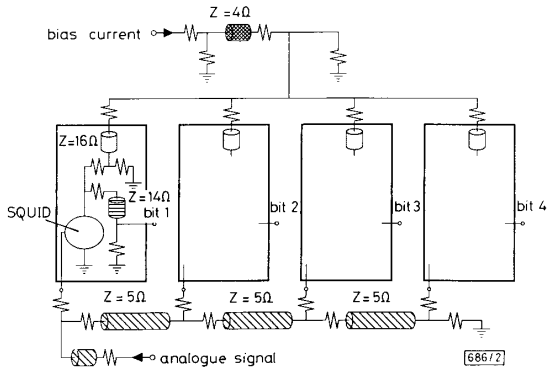

Fig. 2 *Equivalent circuit of designed four-bit A/D convertor*
Circled SQUID represents SQUID shown in Fig. 1