SiGe optoelectronic metal-oxide semiconductor field-effect transistor

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We propose a novel semiconductor optoelectronic switch that is a fusion of a Ge optical detector and a Si metal-oxide semiconductor field-effect transistor (MOSFET). The device operation is investigated with simulations and experiments. The switch can be fabricated at the nanoscale with extremely low capacitance. This device operates in telecommunication standard wavelengths, hence providing the surrounding Si circuitry with noise immunity from signaling. The Ge gate absorbs light, and the gate photocurrent is amplified at the drain terminal. Experimental current gain of up to 1000× is demonstrated. The device exhibits increased responsivity (~3.5×) and lower off-state current (~4×) compared with traditional detector schemes.

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As device dimensions shrink and clock frequencies increase, the volume of chip-to-chip and on-chip communication rockets up. Although still efficient at short distances, copper wires suffer excessive power dissipation and delay in global lines and cannot cope with the growing bandwidth demand [1]. As the chip architecture evolves towards a modular design, the bandwidth density requirements further strain the traditional interconnects [2]. Chip-to-chip and on-chip optical interconnects are promising to alleviate problems faced by copper wires [3]. Compound semiconductors have been the forerunner in optoelectronic applications, but their integration with Si is expensive and hindered by parasitics. Recently, it has been demonstrated that incorporation of Ge into Si is a promising approach that can enable the design of low-cost modulators on Si with potentially higher efficiencies than their hybrid counterparts [4]. This technology is fast approaching to replace the conventional building blocks of the transmitter end in an optical link operating at telecommunication standard wavelengths. Si-based classical optical receivers suffer from large photodiode capacitance; hence they dissipate huge amounts of power besides occupying a large footprint area. Increasingly stringent power requirements on a chip limit the total number of receivers, and hence the number of links.

Optical interconnects can have a great impact in interchip links and on-chip clocking applications. We introduce a novel optoelectronic metal-oxide semiconductor field-effect transistor (OE-MOSFET) for such high-performance applications. The device scales with technology and can be made extremely compact with very low capacitance and small footprint area. By such a design, light can be introduced at the latch level eliminating the ever so power-hungry electrical interconnection hierarchy of clock distribution networks as well as the high-capacitance optical detectors. In this Letter, we demonstrate, with both simulations and experiments, the operation of such a device.

The proposed device is a Si MOSFET with a Ge gate, as depicted in Fig. 1. Source and drain regions are self-aligned to the gate. The signal is generated remotely and is transmitted in the form of optical energy in the 1.3–1.55 μm window, where Ge is a strong absorber. Light can be coupled into the device from the top surface as well as a through waveguide scheme. Incoming photons are absorbed by the Ge gate, and the optically generated carriers move within the gate due to band bending and the applied gate bias, as shown in Fig. 2. This constitutes a net current (I_{GATE}) resulting in accumulation of electrons and holes at either side of the gate insulator. An amplified version of I_{GATE} flows at the drain terminal owing to increased carrier density in the channel. Si, however, is transparent at these wavelengths, so no absorption takes place in the channel; hence the surrounding Si circuitry is noise free, providing noise immunity from clocking and signaling. As light is turned off, the gate oxide capacitance discharges through both increased recombination and diffusion due to the gradient in the carrier concentration. The

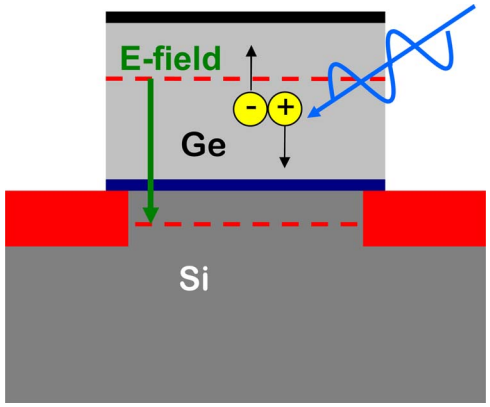

Fig. 1. (Color online) Schematic of the OE-MOSFET. Source/drain and channel regions are formed in Si. The Ge gate is deposited on thermally grown SiO_2. Absorption takes place in the gate. Si is transparent, and hence is noise immune.

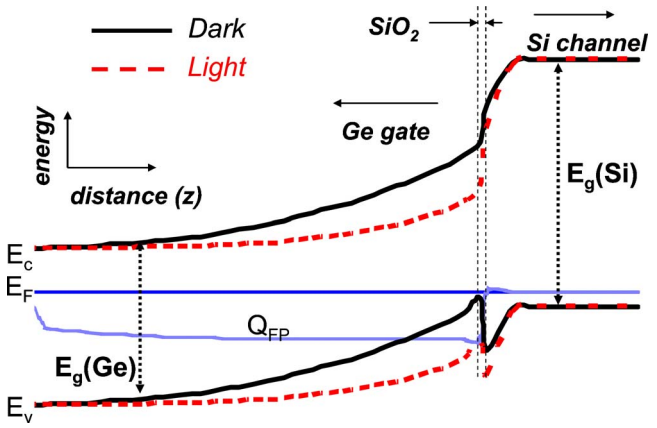

Fig. 2. (Color online) Energy band diagram of the Ge–SiO_2–Si stack. Band bending under equilibrium and steady state illumination are shown by solid and dotted curves, respectively. In the case illustrated here, optically generated holes accumulate at the Ge–SiO_2 interface, while the electrons are swept out of the gate terminal and flow to the SiO_2–Si interface inducing a channel.

overall speed of the device is limited by turn-off, which can be controlled by carrier lifetimes and thickness of the gate region as well as the applied gate bias.

The Ge–SiO_2–Si capacitor governs the operation of the device. Three capacitors are in series: gate depletion, C_{Ge}, insulator, C_{ox}, and channel depletion, C_{Si}. Ge–SiO_2–Si structures are fabricated on (100)-oriented p-type ($\sim 10^{15}$ cm^{-3}) Si wafers. A 3.5 nm thick SiO_2 layer is thermally grown at 900 °C, followed by 240 nm polycrystalline Ge. Gate regions are patterned by photolithography and dry etching. Finally, samples are annealed at 400 °C in forming gas ambient for 45 min. Figure 3 plots the measured capacitance showing the change with light as predicted by simulations. Due to experimental difficulties, visible light is used in capacitance measurements. When $V_{GATE} < -1$ V, the Si channel is accumulated while the Ge gate is inverted. In this region, total capacitance, C_{TOTAL}, is roughly equal to C_{Ge} because C_{ox} is considerably high. Light absorbed in the space charge region modifies the depletion width in the gate, changing C_{TOTAL} and hence the stored charge.

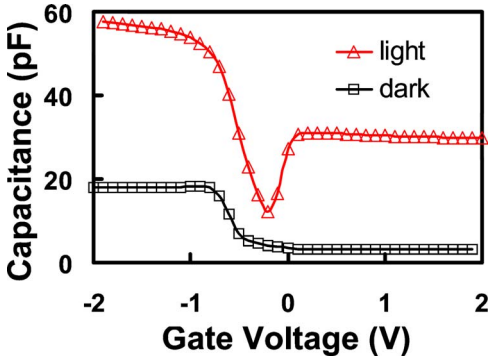

Fig. 3. (Color online) Measured high-frequency (100 kHz) C_{TOTAL}–V_{GATE} for 3.5 nm-thick SiO_2. Due to experimental difficulties, visible light is used in measurements. Si also absorbs at this wavelength, and hence Si depletion capacitance, dominant for $V_{GATE} > 0$, is also modulated.

The accumulation and inversion conditions for Si and Ge are exchanged when $V_{GATE} > 0$ V. Similarly, equivalent capacitance is now dominated by C_{Si} and modified by the light absorbed in the channel.

MEDICI software is used for 2-D electrostatic and transient device simulations. Typical I_{DRAIN}-V_{DRAIN} results obtained by MOSFET simulations are shown in Fig. 4(a). The channel length (L_G) and doping are 1 μm and p-type 10^{18} cm^{-3}, respectively. The input light, 1 $\mu W/\mu m^2$, acts like an additional gate voltage bias modifying the drain current. It should be noted that the transistor gain is not a linear function of the gate voltage owing to the nonlinear relation of I_{DRAIN}-V_{GATE} as shown in Fig. 4(b). Therefore, I_{DRAIN} does not increase linearly with optical power.

Si n-channel MOSFETs are fabricated with a 240 nm polycrystalline Ge gate deposited on 6 nm thick thermally grown SiO_2. Light is coupled into the gate from the top surface. A waveguide coupling scheme can be used in an integrated system application. There is no dc gate current (within measurement noise) due to the insulating SiO_2 layer. An internally modulated 1.55 μm laser with a synchronized lock-in amplifier is used to precisely extract the photocurrent component of the measured signal. The measured gate and drain photocurrents

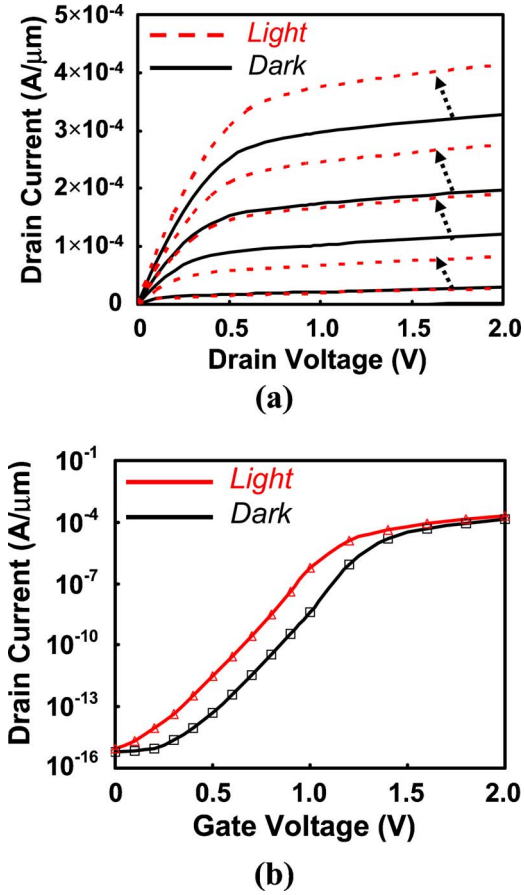

Fig. 4. (Color online) (a) Simulated I_{DRAIN}–V_{DRAIN} results of a 1 μm gate length transistor with n-doped Ge (10^{16} cm^{-3}) and p-doped Si (10^{18} cm^{-3}). Incident light (1 $\mu W/\mu m^2$ in this case) constitutes a gate signal. (b) I_{DRAIN}–V_{GATE} characteristics of the same OE-MOSFET.

versus V_{GATE} for a 100 μm gate length and width transistor are plotted in Fig. 5 for $V_{GATE}=V_{DRAIN}$. The observed drain current is up to 3 orders of magnitude larger than gate current, which can be attributed to the current gain of the transistor. The modulation of channel conductance can further be increased by scaling the gate length, hence increasing the gain. The initial drop in the gate photocurrent is due to transition from gate depletion to accumulation region, similar to that shown in Fig. 3.

Preliminary high-speed characteristics are obtained by transient simulations. Ge is assumed to be a single crystal in the simulations because there are no existing models for the polycrystalline grain boundaries. The grain boundary influence is predicted to reduce the carrier lifetime, thus further increasing the device speed, trading off with sensitivity. The intrinsic speed increases with shrinking gate length. The calculated full width at half-maximum from impulse response simulations are <1 ns and <100 ps for $L_G=1$ μm and $L_G=100$ nm, respectively. The high-speed performance of the OE-MOSFET is benchmarked against that of a traditional photodetector. The response of a classical photodetector to a train of optical pulses is plotted in Fig. 6. The simulated metal–semiconductor–metal has 100 nm electrode spacing on 100-nm-thick Ge. In comparison, the transient response obtained from the OE-MOSFET with an identical 100×100 nm slab of Ge in the gate is also plotted in Fig. 6. This device provides significantly higher photocurrent ($\sim3.5\times$) for identical optical pulse energy in addition to lower off-state leakage ($\sim4\times$). With proper scaling and band engineering, the device is expected to operate easily in excess of 10 GHz. The output capacitance of the device, C_{switch}, is dominated by the gate-to-drain overlap, and it is ~0.02 fF for an OE-MOSFET with 100 nm gate length and width. Therefore, the RC limited bandwidth is very large.

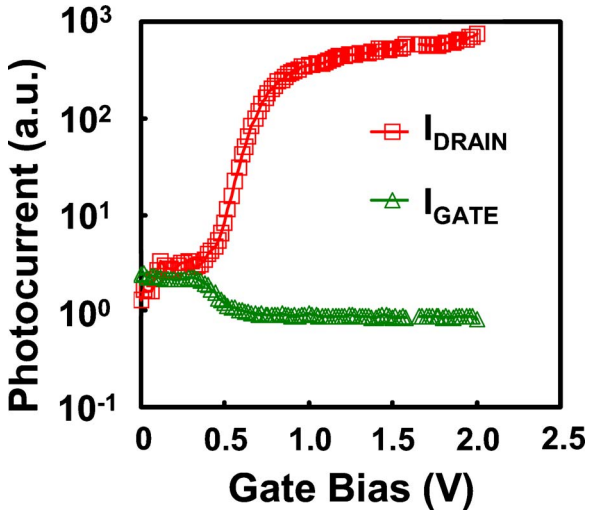

Fig. 5. (Color online) Measured photocurrent at the gate and drain terminals for $V_{GATE}=V_{DRAIN}$. The absorbed light in the Ge gate modulate the conductivity of the Si channel. The gate current is amplified by the transistor at the drain terminal, I_{DRAIN}.

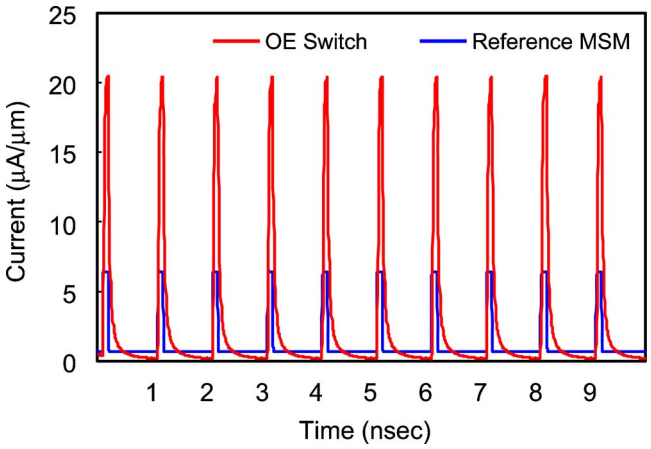

Fig. 6. (Color online) Simulated transient response comparing a classical detector and the proposed device. The input is a pulse train, each pulse delivering 1 fJ optical energy. The OE-MOSFET has significantly enhanced responsivity and lower off-state leakage.

The proposed device essentially is an optical detector with a built-in gain mechanism. In comparison, avalanche photodiodes, for instance, provide gain by impact ionization. However, avalanche photodiodes require high bias voltages (20 V/μm) to achieve desired ionization rates, an increasingly difficult challenge to meet at the operating temperatures of today's processors. In contrast, the OE switch allows low-voltage operation suitable for on-chip applications and potentially better noise performance due to the separation of absorbing and conduction regions.

We have introduced an optoelectronic switch that can be fabricated at the nanoscale along with deeply scaled conventional MOSFETs using advanced Si technology. The device exhibits gain owing to a secondary photoconductive effect based on the current amplification of the field-effect transistor. Such a device has extremely small capacitance and hence can potentially be very fast. The intrinsic speed of the device can be increased by tailoring the carrier lifetimes and built-in band bending using a graded SiGe gate region. Such a switch may be used as an optical latch to distribute an optical clock on chip, eliminating the power dissipation and area due to an H-tree clock distribution network. Plasmonic coupling could be used to focus light on such nanoscale dimensions by nanometallic structures to further enhance device performance [5].

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