

Photonic Crystal Device Optimization Without Increasing Fabrication Tolerances: A Mode Demultiplexer Design

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Abstract: We present a powerful photonic crystal device optimization technique that generates robust designs without requiring precision tuning of device parameters. We optimize the performance of a compact ($8.2 \times 13.3 \mu\text{m}$) waveguide mode demux with the method.

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Currently, the majority of photonic crystal (PC) device designs rely on combining physical insights and innovative modeling with extremely computationally expensive fine tuning. The fine tuning often requires multiple iterations of finite difference time domain (FDTD)[1] or plane wave mode expansion (PWM) calculations[2-4]. Furthermore, improving device performance by fine tuning parameters, such as the geometry within particular lattice sites, is often not practical with current fabrication tolerances. In this paper, we introduce a new optimization method for PC device designs based on Wannier basis analysis and efficient global design optimization by successively enlarging the design space in discrete steps. In our method, allowing only certain modifications to the dielectric distribution, the performance of existing PC device designs can be improved dramatically without increasing fabrication tolerances. By employing a small rank adjustment inverse update procedure, our optimization method is at least 3 orders of magnitude faster than iteratively running FDTD or PWM. We demonstrate our new optimization method by improving the existing design of an extremely compact mode demultiplexer. The device separates the three modes of a input waveguide and converts them into the modes of three single mode output waveguides. As the example will show, the method works even when there is very little physical intuition to guide the optimization. Optimizing PC devices in such a general framework has been computationally impossible until now. Our new method will enable researchers with computing sources of a single personal computer to design PC devices with novel and complex signal processing functionalities.

For clarity, we focus on 2-D PC with TM polarized fields. Extension to the TE case[5] is straightforward. Assume we have a existing PC device design made by introducing defects into the PC, including linear arrays of defects to form the input and output PC waveguides. First, we expand the field in the device in a Wannier basis as $E(\mathbf{r}) = \sum_{n,\mathbf{R}} a_{n,\mathbf{R}} W_{n,\mathbf{R}}(\mathbf{r})$, where $a_{n,\mathbf{R}}$ are the expansion coefficients, $W_{n,\mathbf{R}}(\mathbf{r})$ are the Wannier functions, with Bloch wave band index n and crystal lattice vector \mathbf{R} . Using this expansion in the monochromatic Maxwell's equations and rearranging terms, we get a simple system matrix equation: $\mathbf{B}\mathbf{q} = \mathbf{p}$. In this equation, the system matrix $\mathbf{B} \in \mathbb{R}^{k \times k}$ is calculated from the geometries of the PC defect structure, and \mathbf{p} is a vector describing the input field. \mathbf{q} is a vector of the form $\{\mathbf{r}, \mathbf{t}, \mathbf{a}\}$, where \mathbf{r} , \mathbf{t} are vectors of reflection and transmission coefficients of the input and output waveguide modes. The number of nonzero elements in \mathbf{a} , which represents the field inside the crystal, determines the dimension of \mathbf{B} . This equation can be solved to obtain the transmission/reflection of PC defect structures with PC waveguide input/outputs. The matrix \mathbf{B} is small enough to be inverted directly for structures with as many as 1000 lattice sites. The full form of \mathbf{B} is given in [6]. To improve upon the existing device design, we introduce additional perturbations. It can be shown that, in the presence of an additional dielectric perturbation $\delta\varepsilon(\mathbf{r})$, the system matrix equation changes to

$$(\mathbf{B} + \delta\mathbf{D})\mathbf{q} = \mathbf{p}, \quad (1)$$

$$\text{with } (\delta\mathbf{D})_{n\mathbf{R},m\mathbf{S}} = \int_{\mathbb{R}^2} W_{n,\mathbf{R}}^*(\mathbf{r})\delta\varepsilon(\mathbf{r})W_{m,\mathbf{S}}(\mathbf{r})d^2\mathbf{r}. \quad (2)$$

In our optimization process, we assume that there is a binary choice for the dielectric distribution of each unit cell. Starting with the initial device design, the matrix \mathbf{B}^{-1} is calculated. We define a cost function defined by the sum of the reflection and the unwanted crosstalk powers. Next we try to reduce the cost function by searching through the binary choices for the dielectric distribution of a chosen set of unit cells (i.e., either including or omitting a dielectric rod in each unit cell), using a simulated thermal annealing global optimization technique.

After each step, we find the new transmission/reflection coefficients using Eq. (1). The main computational cost of the optimization is solving Eq. (1) in each search step.

Because we are making large changes to the dielectric distribution at each search step, using a linear approximation to calculate the updated system matrix inverse will not work. We need a method for quickly inverting the updated systems matrix. Let $\delta\mathbf{D}^{(\alpha,i)}$, $\{\alpha = 1,2\}$ be the 2 allowed updates at lattice site i . Due to the localization of the Wannier functions to a few unit cells, $\delta\mathbf{D}^{(\alpha,i)} = \mathbf{X}^{(i)}\mathbf{E}^{(\alpha)}\mathbf{Y}^{(i)}$, where the dimension of $\mathbf{E}^{(\alpha)}$ is very small compared $\delta\mathbf{D}^{(\alpha,i)}$. We dramatically speed up the calculation of $(\mathbf{B} + \delta\mathbf{D}^{(\alpha,i)})^{-1}$ by taking advantage of the small size of $\mathbf{E}^{(\alpha)}$, using an expression for the inverse of a small rank adjustment[7]

$$(\mathbf{B} + \delta\mathbf{D}^{(\alpha,i)})^{-1} = \mathbf{B}^{-1} - \mathbf{B}^{-1}\mathbf{X}(\mathbf{E}^{-1} + \mathbf{Y}\mathbf{B}^{-1}\mathbf{X})^{-1}\mathbf{Y}\mathbf{B}^{-1}. \quad (3)$$

where we have omitted the superscripts for clarity. Despite the longer form, Eq. (3) involves the inversion $\mathbf{E}^{(\alpha)}$ instead of the much larger matrix $\mathbf{B} + \delta\mathbf{D}^{(\alpha,i)}$, and uses \mathbf{B}^{-1} that was already calculated for the initial design. The dimension of $\mathbf{E}^{(\alpha)}$ is typically less than 100, while the dimension of the system matrix \mathbf{B} can be several thousand. Because a matrix inversion has a complexity of $O(n^3)$, using Eq. (3) to find the inverse is at least 3 orders of magnitude faster than direct inversion. This speedup means that simulated annealing based heuristic search has become a computationally practical design method for PC devices.

We demonstrate our optimization method using a mode separator design example. We have designed in [8] a device that separates 3 guiding modes of a multimode waveguide around an operating wavelength of 1503 nm. Compared to previous designs, our design is extremely compact (8.2X13.3 μm) because it does not depend on adiabatic mode transformation[9], or the symmetry of the modes[10]. The mode separator is made by introducing defects into a 2-D PC made of high index cylinders ($n=3.4$, rod radius= $0.18a$, a =lattice constant) in air. The input waveguide made of three rows of missing rods supports three modes. The 3 output single mode waveguides are made of single rows of missing rods. The mode separator takes the 3 modes of the input guide and separates them into the three output waveguides. For reference, the mode separator design and its transmission characteristics are show in Fig. 1.

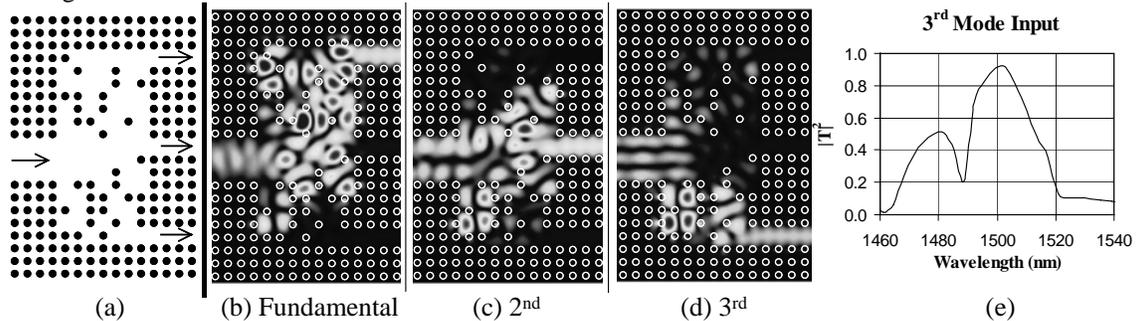


Fig. 1. (a) Design of the mode separator. Dark circles represent high index rods in air. The PC parameters are given in the text. Arrows shows the input and output ports. (b, c, d) Mode separator in action. The three field patterns are for each of the three input waveguide modes. Lighter shading indicates larger field. The structure is superimposed onto the field patterns. The irregularities in the input fields are due to the small reflections (-10dB) from the device. (e) Transmission power spectrum on the intended output port for 3rd mode input.

We see from Fig. 1(e) that the peak transmission for the original design is ~90%. Ideally we would like to increase this figure to 100%. We could fine tune the device design by perturbatively changing the radius or the dielectric constant of the rods. However, accurate control of individual rod radius is challenging with current fabrication technology, and arbitrary dielectric constant over a large range is difficult to realize. Instead, we will try to improve the design using a perturbation that is easily realizable in fabrication. More specifically, in the first optimization step, we will remove or add the high index rods forming the PC, in the boxed region #1 shown in Fig. 2(a). The complete removal of a rod is much easier to accomplish in fabrication that trying to control the radius of a rod. However, complete removal of a rod dramatically changes the device characteristic, and any perturbative analysis would be highly inaccurate. Therefore, we use Eq. (3) to calculate the new transmission/reflection. In the second step, we optimize the rods in box #2. Repeating the process, the device performance is improved by successively stacking layers of perturbation to the output of the device.

It should be pointed out that, if FDTD simulations are used, roughly 10 hours would be needed on a Pentium 4 computer to find the change in the transmission for the addition or removal of one rod. In contrast, our method took roughly 3 seconds to compute effect of adding or removing a rod. Finding the optimized device, where we calculated the effect of over 10000 possible perturbation scenarios, would be extremely computationally expensive

for FDTD. It should be pointed out that, before starting the optimization, we needed roughly 10 minutes of computation time to calculate the perturbation matrix $\delta\mathbf{D}$ for perturbation to a single unit cell. This matrix, however, only needs to be calculated once.

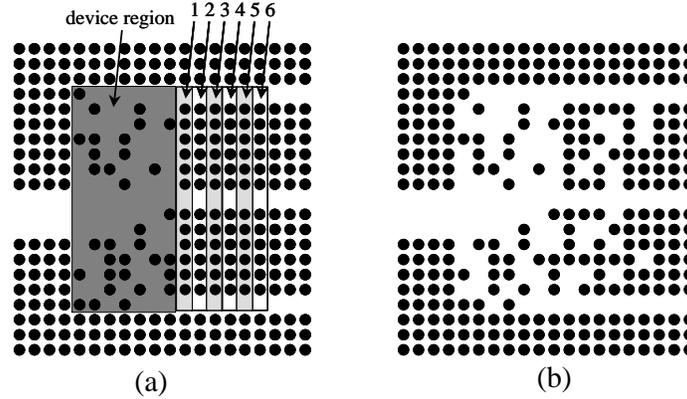


Fig. 2. (a) Device before optimization. The numbered boxes represent the regions and the order to which the optimization is applied. The existing device region is not changed in the optimization. (b) Final device after optimization

Fig. 2(b) shows the device after optimization. Fig. 3 compares the device performance before and after optimization. We can see that the device characteristics, especially the transmission into the desired output at 1500 nm, are greatly improved compared to the initial design. We emphasize that the rods in the optimized structure all have the same radius. The simple geometry makes the design much easier to fabricate.

Compared to coupled mode methods, our Wannier based analysis is accurate and efficient even when there is very strong coupling between defect sites. As a result, we can efficiently analyze and optimize regions very close to the original device. From Fig. 2(b), we see that optimization introduced isolated defect sites in the numbered boxed regions. However, because the boxed regions are next to each other, the isolated defects are not strongly confined. This means that the isolated defects will not introduce sharp unwanted spectra features. This is apparent from Fig. 3. In conclusion, we have demonstrated that combining Wannier basis analysis with small rank adjustment optimization gives a powerful tool for optimizing PC devices designs without increasing fabrication tolerances.

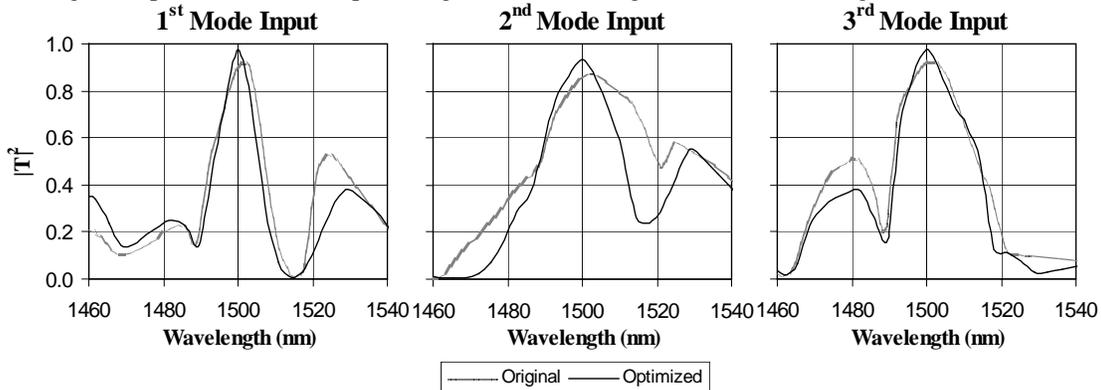


Fig. 3. Power transmission spectra at the intended output ports for 3 input modes. The original and the optimized spectra correspond to structures shown in Fig. 2(a) and (b) respectively. The peak transmission is improved in the optimized structure without significant degradation to the bandwidth.

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