

## 18.2 A 20GHz Bandwidth, 4b Photoconductive-Sampling Time-Interleaved CMOS ADC

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High speed analog-to-digital converters capable of digitizing signals with bandwidths of several tens of GHz have applications in high-speed instrumentation, wideband radar and optical communications. However, the design of converters with such high input bandwidths is constrained by the need for wideband sample-and-hold circuits with sufficiently low clock jitter. A number of photonic sampling techniques have been proposed to overcome the limitations of conventional electronic sampling circuits [1]. This work introduces a parallel ADC architecture, shown in Fig. 18.2.1, wherein a large number of time-interleaved photonic sampling channels each feed a 4b, 1GS/s CMOS ADC. The electrical input is sampled onto a hold capacitor using low-temperature-grown (LT) GaAs photoconductive switches that are optically triggered by a mode-locked laser generating sub-picosecond wide pulses at a 1GHz repetition rate. The output of the laser is split into multiple phase-delayed beams to drive the time-interleaved LT GaAs switches. The switches provide a sampling aperture of a few picoseconds with almost 6 bits of linearity and a sampling bandwidth greater than 50GHz [2]. The 4b ADC used to digitize each of the sampled signals is constrained by the need for a very low input capacitance and a small area, the latter necessary to allow the integration of many converters on a single chip to maximize the aggregate sampling rate. The use of optically triggered sampling and interleaving relaxes the jitter, timing skew and speed requirements of the electronic ADC's.

LT GaAs has a short carrier lifetime of only a few picoseconds and is highly resistive except when illuminated. Incident light generates excess electron-hole pairs that enable conduction, but these carriers recombine within a few picoseconds after the light is removed, providing a very fast response. The LT GaAs switch consists of a planar 8-finger metal-semiconductor-metal (MSM) pattern in a 20 $\mu$ m by 20 $\mu$ m area. The switch provides a peak on-resistance  $R_{ON} < 100\Omega$  and an off-resistance  $R_{OFF} > 100M\Omega$  but exhibits considerable capacitive feedthrough of approximately 10fF. A replica dummy switch is used in a differential architecture to cancel this feedthrough. The photoconductive switches are flip-chip bonded to the CMOS chip and illuminated from the back side. With a 30fF hold capacitance, the switches provide a sampled output of 0.4V<sub>pp</sub> differential with a common-mode signal of 0.35V<sub>pp</sub> when sampling a 0.56V<sub>pp</sub> input.

Shown in Fig. 18.2.2 is a block diagram of the CMOS ADC. The differential buffer amplifier rejects the common-mode input and provides a linear differential gain of 4 to drive the flash quantizer with a full-scale range of 1.6V<sub>pp</sub> differential. The quantizer consists of 15 main comparators with an additional 6 dummy comparators for averaging random nonlinearities [3]. The averaging resistors reduce the INL by a factor of 2.2. An externally adjustable current is used to calibrate the ADC offset.

A schematic of the input buffer is shown in Fig. 18.2.3. To remove memory of the previous sample, the sampled input is reset prior to photoconductive sampling. Both sample and dummy signals are buffered by low input capacitance PMOS source-followers.

Mismatch in the small PMOS transistors is the main source of amplifier offset. A linear transconductance amplifier (shown in dashed lines) rejects input common-mode while providing a fixed differential voltage gain set by resistor and current mirror ratios [4]. The buffer amplifier settling time limits the maximum sampling rate of the CMOS ADC.

The regenerative preamplifier shown in Fig. 18.2.4 provides approximately 4V/V of differential gain in 200ps of regeneration time. Cross-coupled MOS capacitors cancel feedback through the gate overlap capacitance that may otherwise distort the input. A low-offset, low-swing comparator follows the preamplifier to provide additional regenerative gain, and the latch array amplifies the main comparator outputs to CMOS voltage levels. The thermometer code output of the latches drives a 4b ROM that produces the corresponding binary output code.

Shown in Fig. 18.2.5 is a die micrograph of a prototype two-channel A/D converter fabricated in a 0.25 $\mu$ m CMOS process with flip-chip bonded LT GaAs switches. Each channel occupies 150 $\mu$ m by 450 $\mu$ m area and consumes 70mW of power, not including output drivers, at a sampling rate of 1GS/s. With a low-frequency signal applied directly to the CMOS ADC inputs, the measured INL and DNL of both channels is less than 0.2 LSB and 0.25 LSB, respectively. The measured gain and offset mismatch of the two channels, before calibration, was 1.5% and 62mV (0.62 LSB), respectively.

Photoconductive sampling measurements were carried out using a 150fs pulse-width, 80MHz repetition-rate, mode-locked laser with a phase-locked electrical pulse generator at frequency  $f_{CLK}$  driving the CMOS ADC's. The test setup was limited to a sampling rate  $f_s = 80MS/s$ , but the CMOS ADC was operated at  $f_{CLK} = f_s, 4f_s$  and  $8f_s$ , to verify its operation at higher clock rates. For  $f_{CLK} = 4f_s$  and  $8f_s$ , the ADC outputs are subsampled by a factor of four and eight, respectively. The high-frequency input signal was driven directly onto the chip using Ground-Signal-Ground microwave probes. Fig. 18.2.6 shows a plot of the peak SNDR and corresponding SFDR of one channel measured over input frequencies from 3MHz to 20GHz. The SFDR improves as frequency increases because common-mode feedthrough of the photoconductive switch is attenuated by the buffer amplifier's limited bandwidth. The peak SNDR remains approximately constant up to 20GHz input frequencies and does not appear to be limited by jitter from the laser or the input source. Testing of the simultaneous operation of both channels, as well as operation at 1GS/s sampling rates, is in progress. Fig. 18.2.7 summarizes measured results.

### Acknowledgements

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### References

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- [2] R. Urata et al., "High-Speed Sample and Hold Using Low Temperature Grown GaAs MSM Switches for Photonic A/D Conversion," Conference on Lasers and Electro-Optics, talk CMN4, May 2001.
- [3] K. Kattmann and J. Barrow, "A Technique for Reducing Differential Non-Linearity Errors in Flash A/D Converters," *ISSCC Digest of Technical Papers*, pp. 170-171, Feb. 1991.
- [4] M. Koyama et al., "A 2.5V Active Low-Pass Filter Using All npn Gilbert Cells with a 1-V<sub>pp</sub> Linear Input Range," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1246-1253, Dec. 1993.

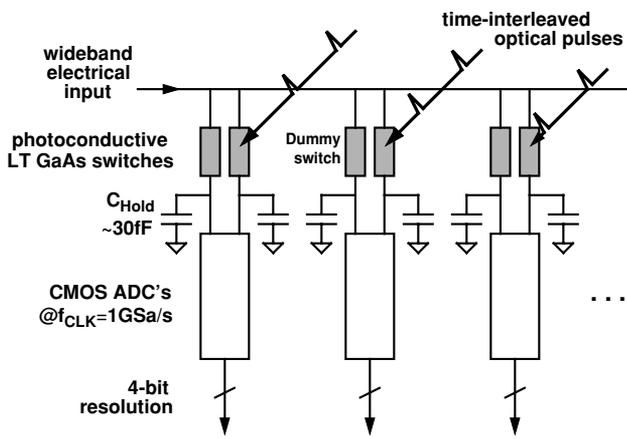


Figure 18.2.1: Proposed ADC architecture.

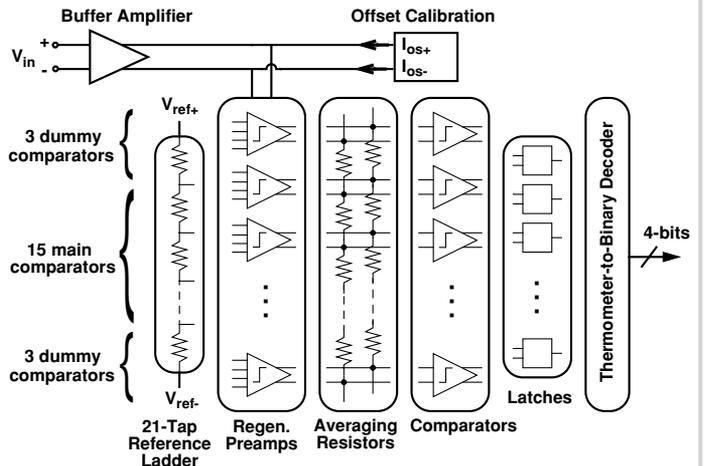


Figure 18.2.2: Block diagram of CMOS ADC.

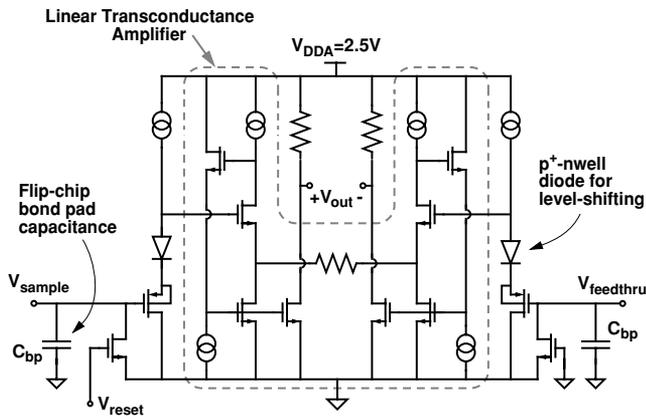


Figure 18.2.3: Schematic of input buffer amplifier.

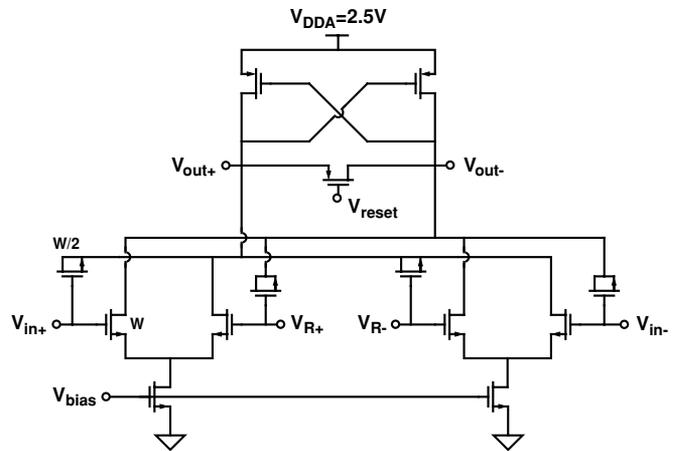


Figure 18.2.4: Schematic of regenerative preamplifier.

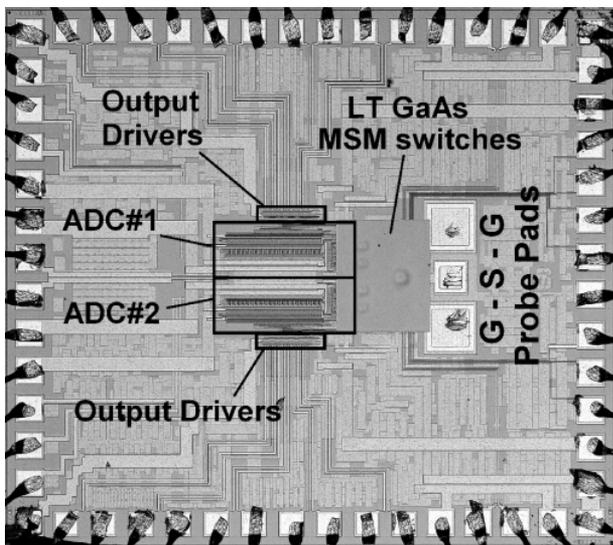


Figure 18.2.5: Chip micrograph.

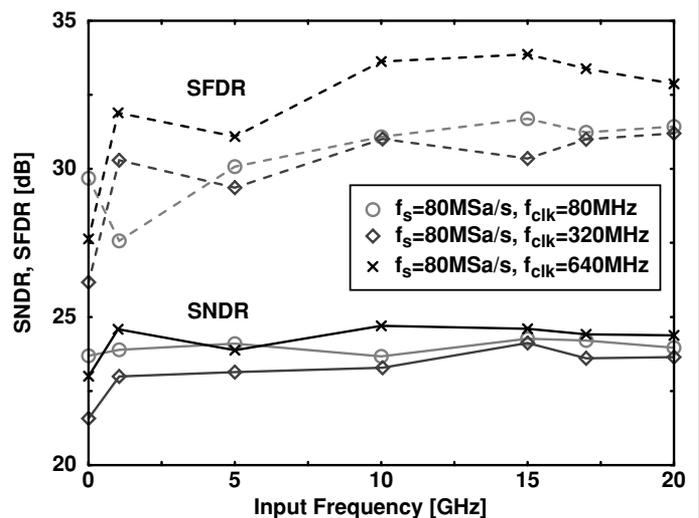


Figure 18.2.6: Peak SNDR and SFDR versus Input Frequency.

Technology	1-poly 5-metal 0.25- $\mu\text{m}$ CMOS w/ LT GaAs
Supply Voltage	2.5 V
Number of time-interleaved channels	2
Sampling Rate per channel	80 MSample/s
Nominal Resolution	4 b
Input Range	560 mV peak-to-peak
Peak SNDR (@ $f_{in}=20\text{GHz}$ ) of one channel	23.9 dB
SFDR (@ $f_{in}=20\text{GHz}$ ) of one channel	31.4 dB
DNL	< 0.2 LSB
INL	< 0.25 LSB
Active area per channel (excl. output drivers)	150 $\times$ 450 $\mu\text{m}^2$
Power Dissipation per channel	
Analog	40 mW @ $f_{CLK} = 640 \text{ MHz}$
Digital (excl. output drivers)	30 mW @ $f_{CLK} = 640 \text{ MHz}$
Optical	~5 mW @ $f_S = 80 \text{ MSample/s}$

Figure 18.2.7: Performance summary.

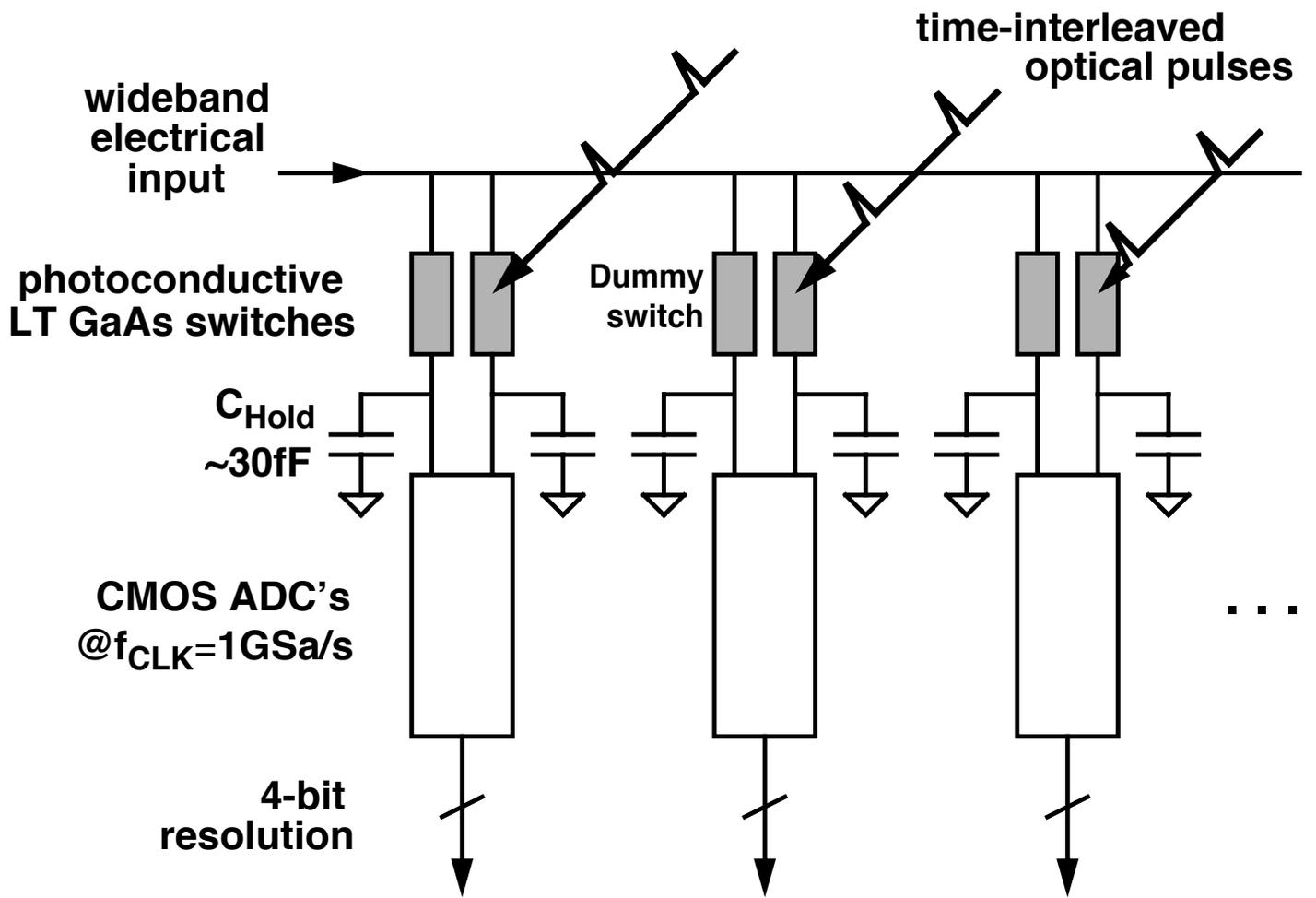


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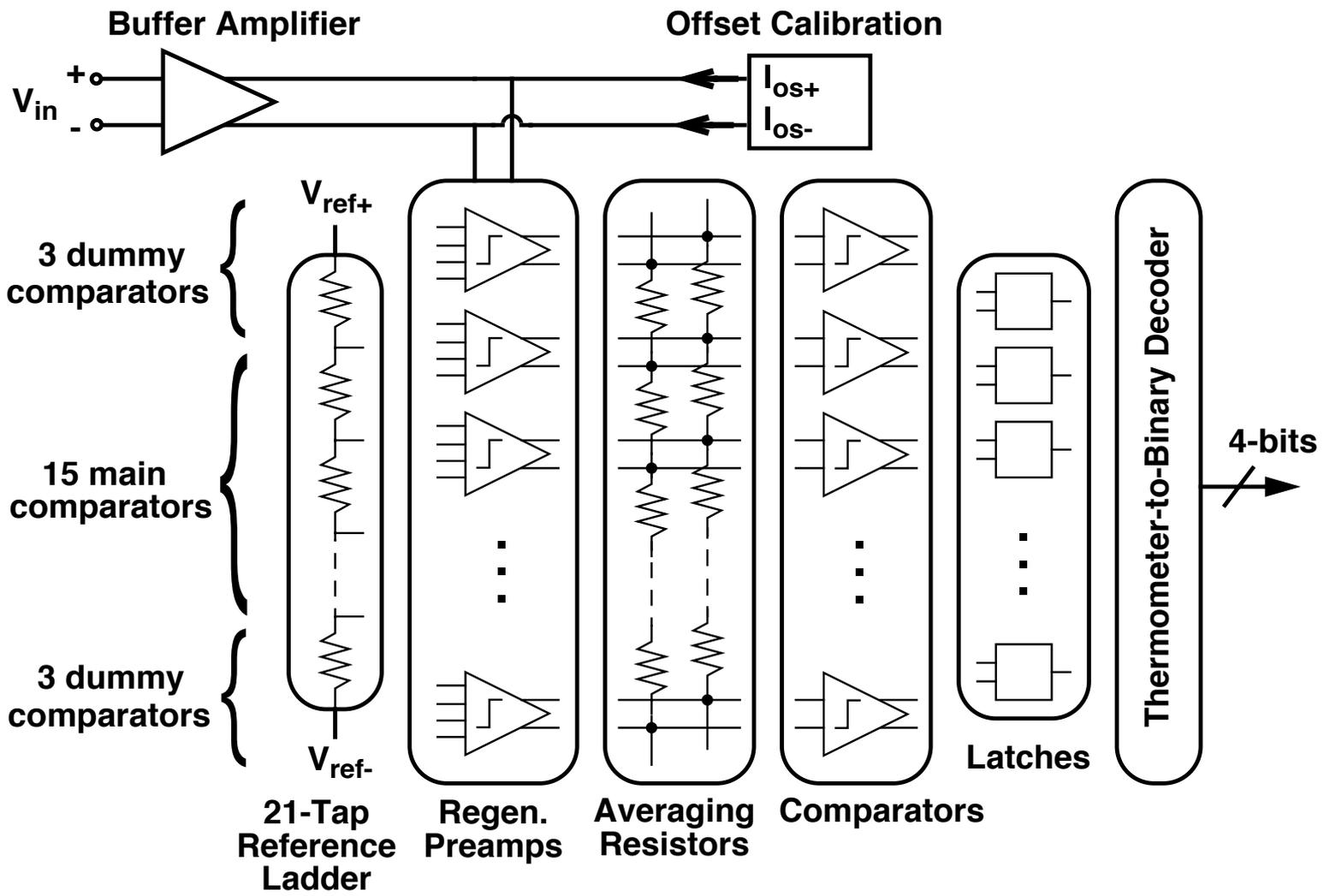


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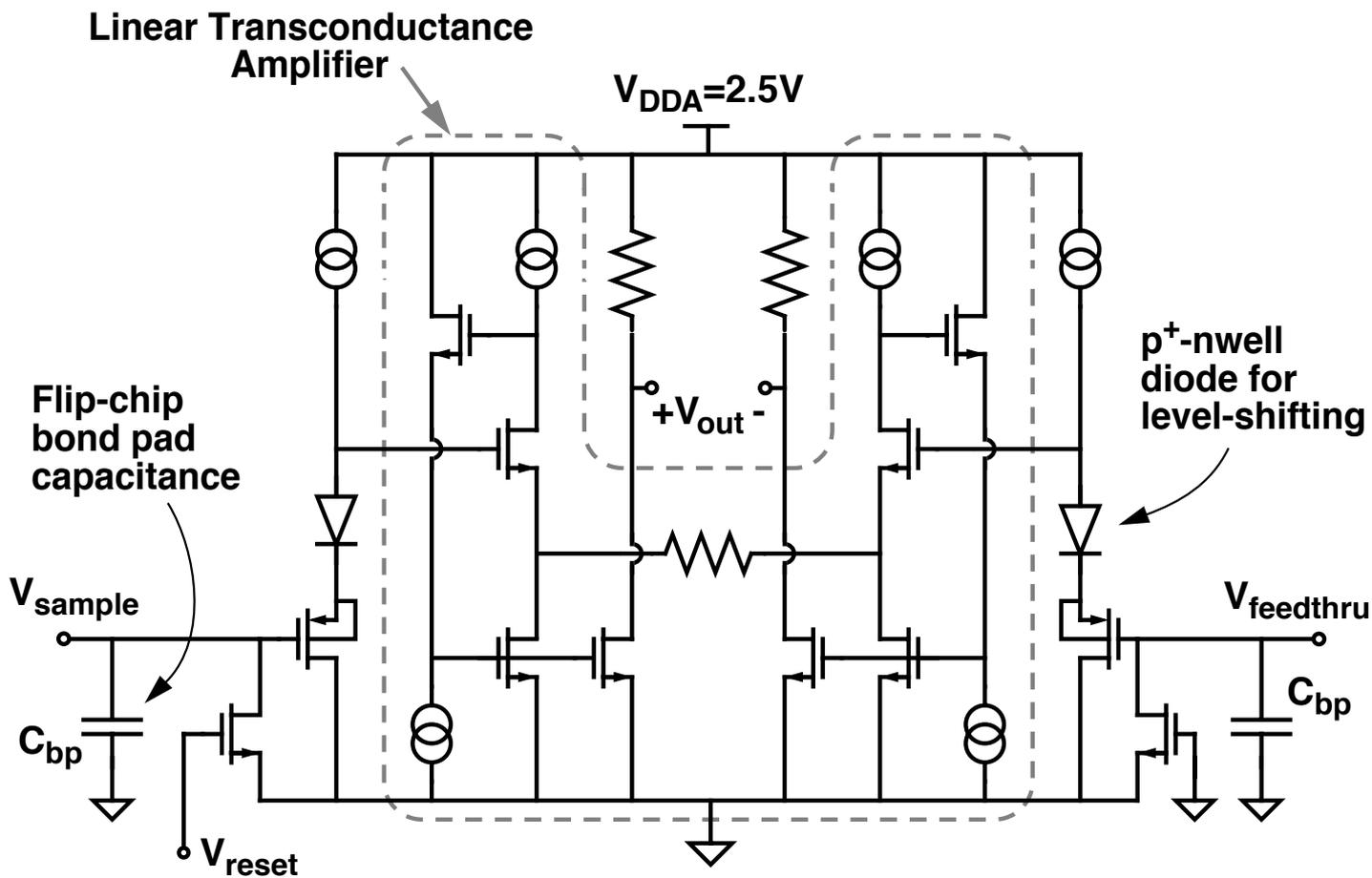


Figure 18.2.3: Schematic of input buffer amplifier.

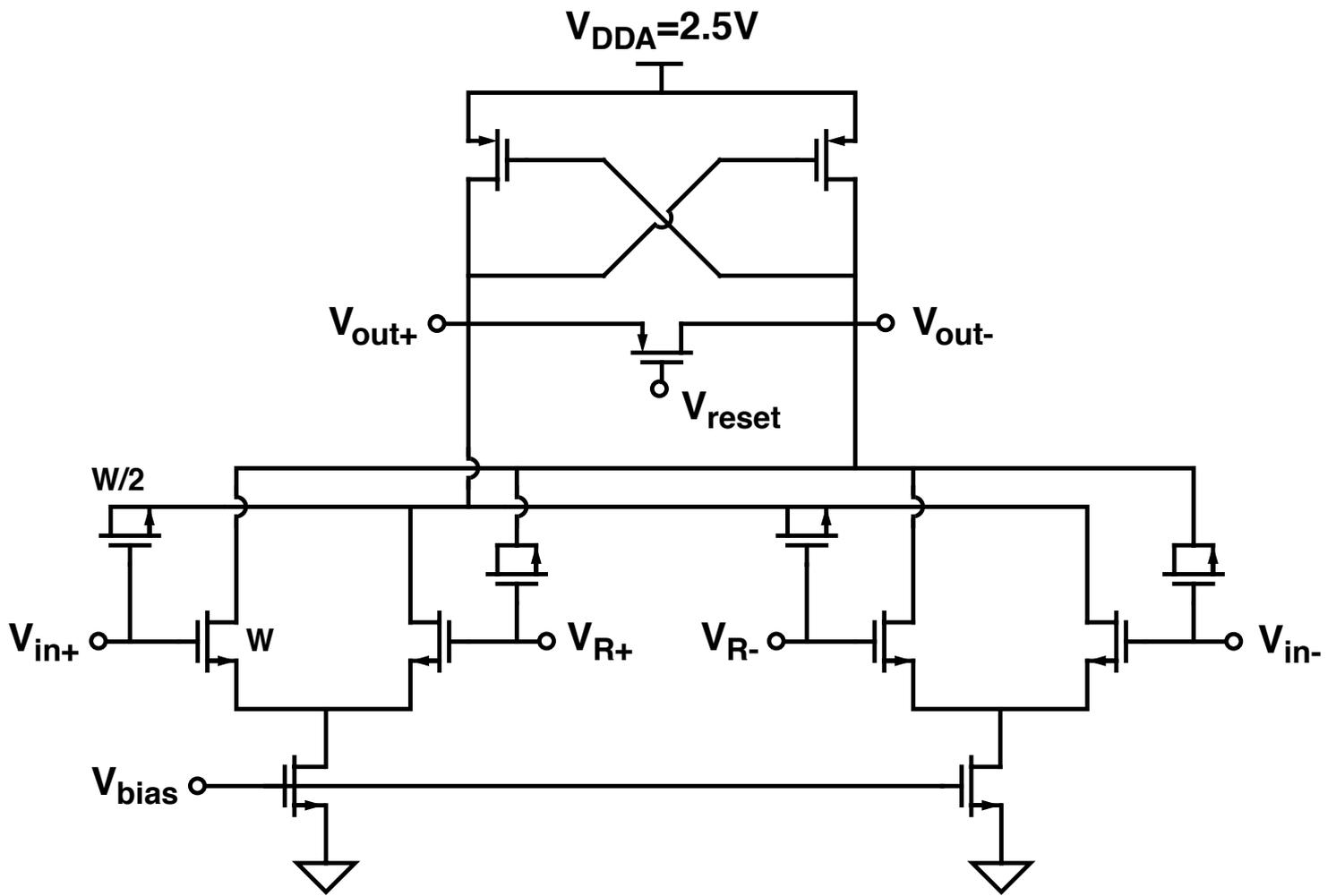


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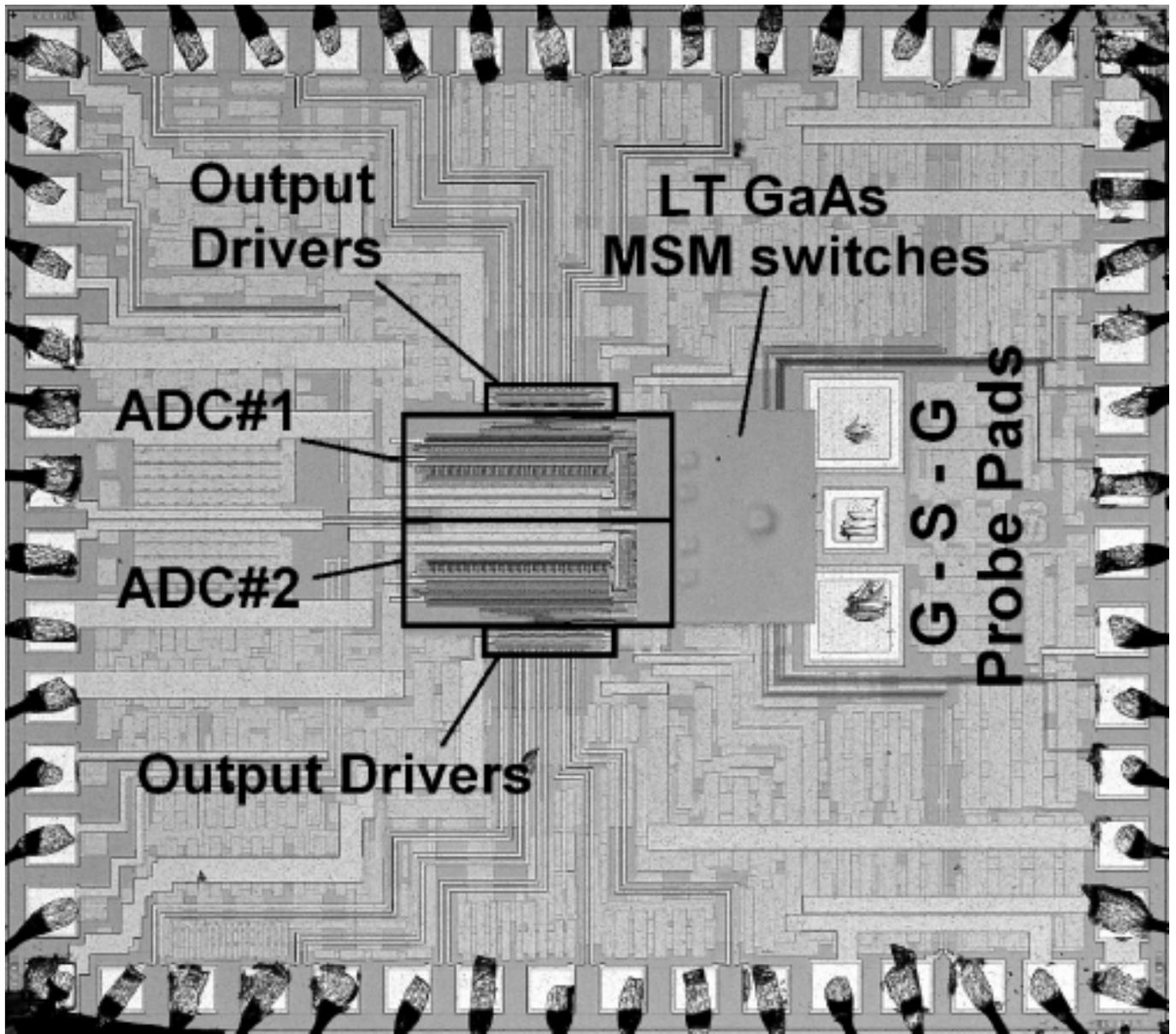


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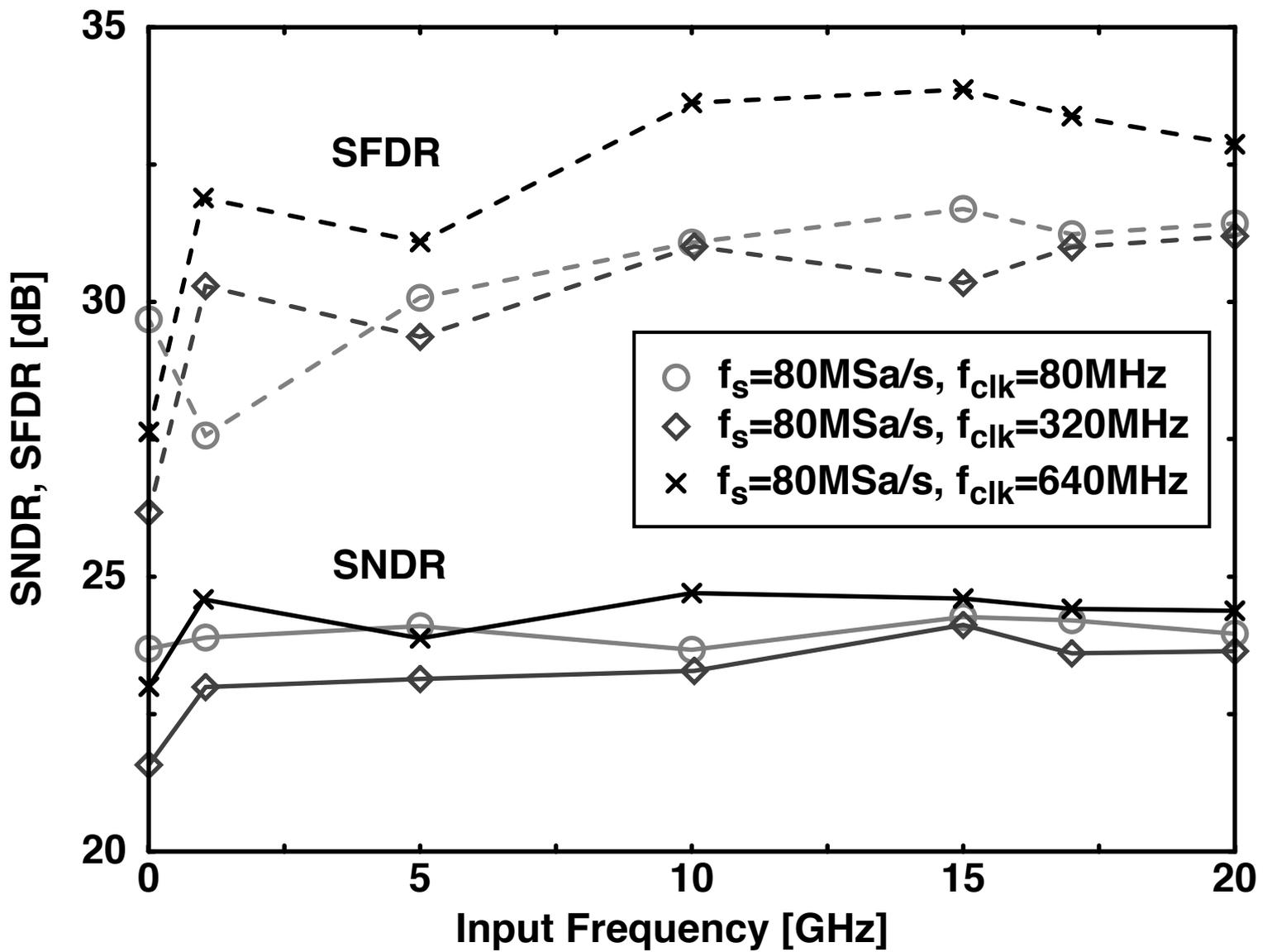


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<b>Sampling Rate per channel</b>	<b>80 MSample/s</b>
<b>Nominal Resolution</b>	<b>4 b</b>
<b>Input Range</b>	<b>560 mV peak-to-peak</b>
<b>Peak SNDR (@<math>f_{in}</math>=20GHz) of one channel</b>	<b>23.9 dB</b>
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<b>DNL</b>	<b>&lt; 0.2 LSB</b>
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<b>Power Dissipation per channel</b>	
<b>Analog</b>	<b>40 mW @ <math>f_{CLK}</math> = 640 MHz</b>
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