SP 25.5: 15μm Solder Bonding of GaAs/AlGaAs MQW Devices to MOSIS 0.8μm CMOS for 1Gb/s Two-Beam Smart-Pixel Receiver/Transmitter

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A two-beam optical repeater circuit operates to 1Gb/s, consumes 10mW, occupies about 1100μm², and is realized with a technology capable of providing thousands of optical inputs and outputs to foundry-grade VLSI silicon CMOS circuitry. The technology provides this capability by attaching GaAs/AlGaAs multiple-quantum-well (MQW) modulators and detectors to VLSI CMOS with flip-chip solder bonding [1]. A detailed discussion of the process is available elsewhere, but the main unique features can be summarized here [2, 3]. First, the commonly held image of a flip-chip-bonded assembly in which the surface of the Si die is inaccessible is invalid, because the GaAs substrate supporting the MQW devices is removed after bonding, leaving individually pixellated devices. Second, the solder bond is 15x15μm², reducing the parasitics of the connection. Finally, the solder-attachment pads can be placed in the top-level interconnect metal of the silicon circuit, permitting a three-dimensional integration in which active CMOS circuitry is present underneath the attachment pads [4]. Chips containing about 140,000 FETs and 4352 fully-functional MQW diodes have been demonstrated [5]. Clearly, key elements of such a technology are the receiver and transmitter circuits interfacing between the optics and the electronics. There is a premium placed on small, low-power consumption elements. Multiple-beam receivers are reasonable candidates, because it may be assumed that information transport is over a relatively short distance. The two-beam receiver may have certain advantages in common-mode dynamic range and noise immunity over single-beam receivers [6].

Several receiver designs, fabricated in MOSIS 0.8μm CMOS, work to data rates in the 1Gb/s range. One example is shown in Figure 1, with FET widths in microns indicated (lengths were all 0.8μm). An idealized cross-section of the technology is shown in Figure 2, with a micrograph of part of a test chip appended. Although many first-stage amplifier topologies can be considered, an inverter is selected for simplicity, power, and size. With straight forward layout, the entire circuit fits in 45x25μm², reducible to 30x30μm² with aggressive packing. The output voltage of the receiver in each logical state (k=0,1) is determined by the difference in optical power δP_k = P1 - P2 falling on the two detectors shown in Figure 1, through the corresponding photocurrent difference δi_k. It is clearly desirable for the receiver to have a symmetric response to ±δP, which explains many of the design choices. Loading associated with a fully bonded and wired MQW diode is 50-60fF [7].

Several feedback topologies have been studied. Both types employ a p-type FET as a replacement for the textbook feedback resistor, as mentioned in Reference 8, while in type B this is augmented with diode-connected n-FETs. Since this was the first design effort, a tuning voltage was applied to the gate of the feedback FET for control of the transimpedance gain. Simulations indicate that the transimpedance gain of the first stage is varied between 160kΩ at 155Mb/s and about 5 kΩ at 1Gb/s by this tuning voltage. The second stage of the receiver consists of another inverter-based gain stage, now using diode-connected FETs on the output acting to broaden the switching transition of the inverter while maintaining a transition point equal to that of the first stage. This is a variation on a common preamplifier design used in single-beam photoreceivers[4]. These diode-connected FETs symmetrically broaden the gain region of the amplification stage (this would not be the case if only one diode-connected FET were employed, for example). Subjectively, it is found that while receivers with a second stage that omits these load elements work, they are more susceptible to oscillation, reduced dynamic range, and unbalanced operation. The third stage of the receiver is an inverter. The output of the receiver is connected to a transmitter circuit (see Figure 1 to the right of the dashed line) driving two MQW modulator devices that encode data on light beams reflected off of them.

The performance of the repeater is presented in Figures 3, 4, and 5, which show an eye pattern, an input/output bit pattern at 1Gb/s, and power and sensitivity data as a function of bit rate, respectively. Bit-error-rate measurements at the 10^{-9} level determine the sensitivity data in Figure 5. The receiver with type A feedback is capable of higher-speed operation than that of type B, which is attributed to the large feedback FET employed in the type B circuit (8μm wide) and the associated loop capacitance. The amount of variation of input optical power tolerable with $\delta P_1 = -\delta P_0$ is also measured. At 622Mb/s, this common-mode dynamic range exceeded the maximum 16dB that could be provided in the testing system, and at 155Mb/s it exceeded 20dB. This is not surprising, since the receiver operates in a balanced fashion. As expected, little relative variation between the two beams is tolerable. Finally, the susceptibility of the receiver to power-supply noise has been studied. By placing a bias tee in the Vdd supply line, uncorrelated 50MHz sine waves can be superimposed on Vdd, and eye patterns observed. When operated at twice the minimum input photo-current (e.g., 2μA at 311 Mb/s) eye pattern degradation is seen at 200-300mV of injected noise. It is clearly advisable to insulate such a receiver as much as possible from the high-supply-noise environment characteristic of digital CMOS, perhaps by using separate supply lines and greater-than-minimum input optical powers. For all measurements Vdd is 5V, detector biases are +12 and -10V, modulator biases are +11V and -6V, and V_{tune} is adjusted for optimum sensitivity at given bit rate.

Power consumption of the type B repeater is shown in Figure 5, taken by measuring the current in a dedicated 5V supply. Simulations indicate that the transmitter contributes roughly 2mW to this power, so the approximate power consumption of the receiver itself is 8mW. The dissipation decreases as the bit rate increases, indicating that static power dominates. To enable thousands of such receivers on a single chip, the power consumption of the smart-pixel receiver must be further reduced. Given the comparatively huge footprint and power consumption of an electrical off-chip CMOS driver capable of supporting 622Mb/s data rates, these values of power consumption are still attractive. The power and sensitivity of this receiver could be further optimized for specific system applications. Figure 6 is a test chip micrograph.

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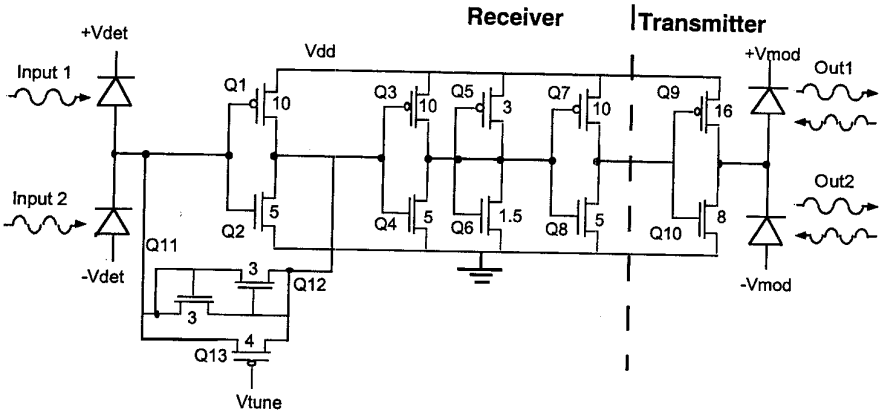

Figure 1: Circuit schematic. FET widths in microns, lengths all 0.8μm, feedback topology B illustrated, topology A omits Q11 and Q12 and makes Q13 8 μm wide. Diodes are solder-bonded 15x45μm² MQW devices.

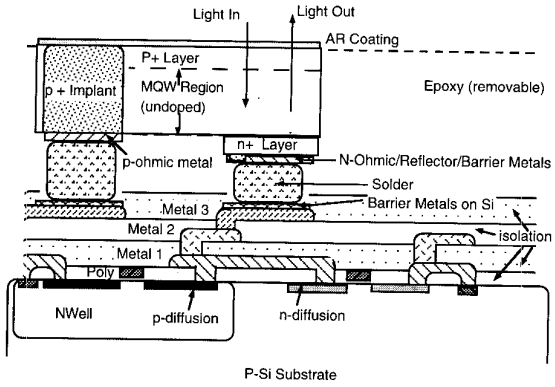

Figure 2: Cross section of integration (not to scale).

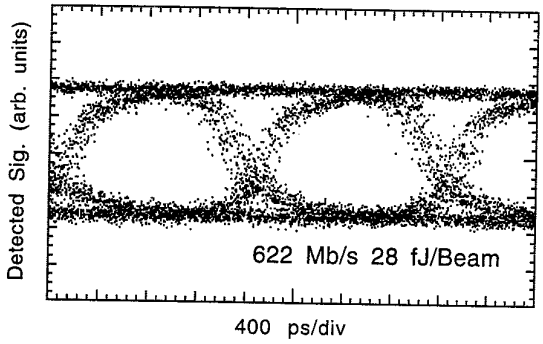

Figure 3: Eye pattern at 622Mb/s acquired for 10s.

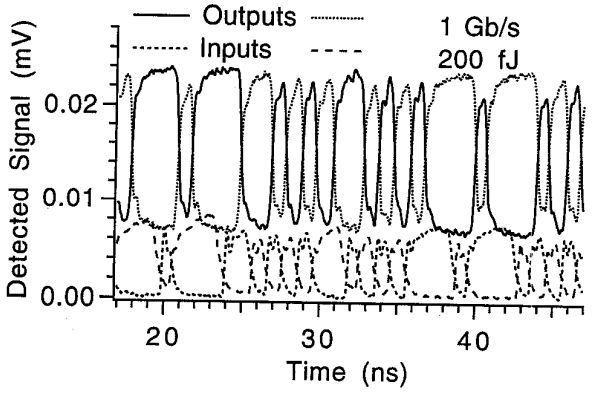

Figure 4: Input/output at 1 Gb/s. Inputs from directly modulated 850nm laser diodes and outputs taken optically from two MQW modulators. Timing and output contrast ratio correctly represented.

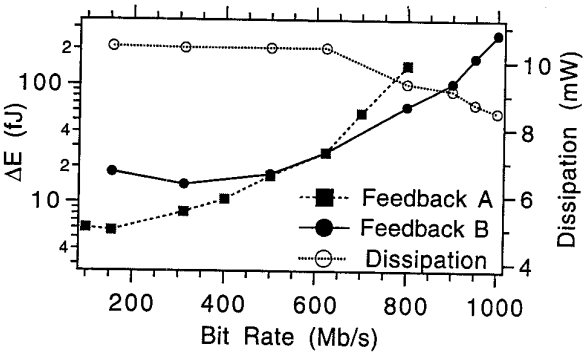

Figure 5: Optical pulse energy in each beam for two feedback topologies (left axis, solid symbols) and electrical power consumption of Type B feedback topology (right axis, open symbols) vs. bit rate. Points are 10^{-9} measured bit error rate with 2^{23}-1 pseudo-random-bit sequence.

Figure 6 and *References*: See page 482.

(Continued from page 407)

References:

[1] A mutliple-quantum-well modulator is a p-i-n diode whose near-bandedge absorption is voltage dependent, yielding an absorption modulator. For more information, see, D. A. B. Miller, Optical and Quantum Electronics, 22, pp. S91-S98, 1990.

[2] Goossen, K., et.al., "GaAs MQW Modulators Integrated with Silicon CMOS," IEEE Photon. Tech. Lett., 7, No. 4, p. 360, April, 1995.

[3] Krishnamoorthy, A. V., et. al. "3-D Integration of MQW SEED Modulators over Active Sub-Micron CMOS Circuits: 375 Mb/s Transimpedance Receiver-Transmitter Circuit," to appear IEEE Phot. Tech. Lett.

[4] Krishnamoorthy, A. V., et. al., "Implementation of a Photonic Page Buffer Based on GaAs MQW Modulators Bonded Directly Over Active Silicon VLSI Circuits," Proc OSA Topical Meeting on Optical Computing, Paper PDP-2, March, 1995.

[5] Lentine, A. L., et al., "Demonstration of an experimental single chip optoelectronic switching system," Postdeadline paper PD2.5, 1995 IEEE LEOS, Oct. 31, 1995.

[6] For more information, see, for example, T. K. Woodward, L. M. F. Chirovsky, "Operation of Diode-clamped FET-SEED Optical Receivers with Low-Contrast Single-Ended Signals", to appear in IEEE Phot. Tech. Lett, or T. K. Woodward, A. L. Lentine, L. M. F. Chirovsky, "Experimental Sensitivity Studies of Diode-Clamped FET-SEED Smart Pixel Optical Receivers," IEEE J. Quant. Electr., Vol. 30, No. 10, pp. 2319-2324.

[7] For more information on this see A. V. Krishnamoorthy, et. al. "Ring Oscillators with Optical and Electrical Readout Based on Hybrid GaAS MQW Modulators Bonded to 0.8 μm Silicon VLSI Circuits," Submitted to Electronics Letters.

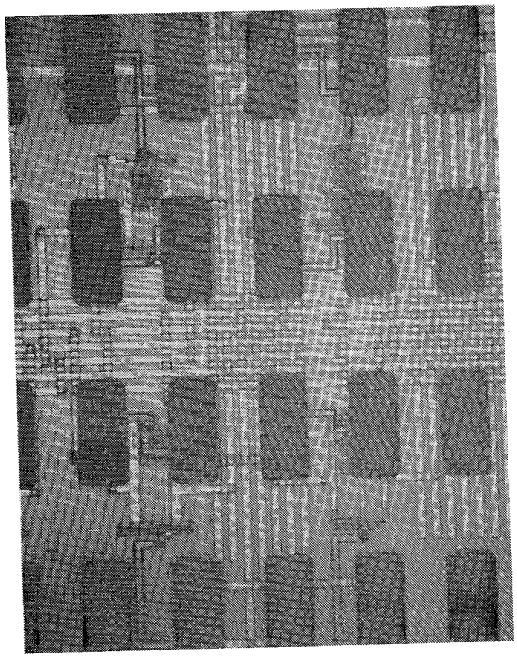

Figure 6: Part of tester chip with receivers and transmitters & MQW bonded devices (dark areas are circuits).

SP 25.6: A Millimeter-Wave Flip-Chip IC using Micro-Bump Bonding Technology

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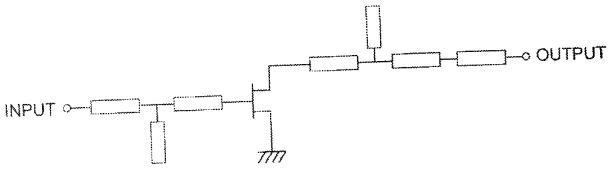


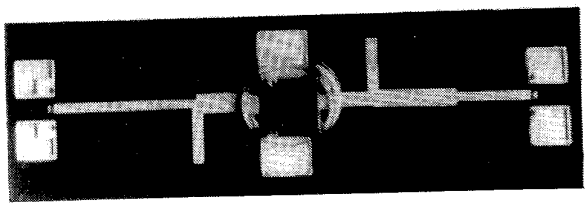
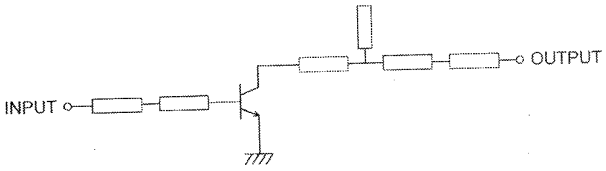


Figure 5: Schematic and micrograph of 50GHz-band MFIC amplifier using HFET.



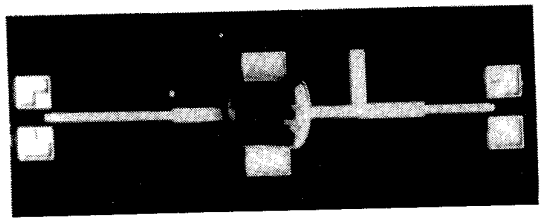


Figure 6: Schematic and micrograph of 50GHz-band MFIC amplifier using HBT.