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Novel planarization and passivation in the integration of III-V semiconductor devices

Jun-Fei Zheng*[a], Jesper Hanberg[b], Hilmi Volkan Demir[c], Vijit A. Sabnis[c], Onur Fidaner[c], James S. Harris, Jr[c]., David A. B. Miller[c]
[a]Intel Corporation, SC1-05, 3065 Bower Ave, Santa Clara, CA, USA 95052
[b] GiGA ApS, an Intel Corporation, Skv1,Mileparken 22, DK-2740 Skovlunde, Denmark
[c]E.L. Ginzton Laboratory, Solid State and Photonoic Laboratory, Stanford University, Stanford, CA USA 94306

ABSTRACT

III-V semiconductor devices typically use structures grown layer-by-layer and require passivation of sidewalls by vertical etching to reduce leakage current. The passivation is conventionally achieved by sealing the sidewalls using polymer and the polymer needs to be planarized by polymer etch-back method to device top for metal interconnection. It is very challenging to achieve perfect planarization needed for sidewalls of all the device layers including the top layer to be completely sealed. We introduce a novel hard-mask-assisted self-aligned planarization process that allows the polymer in 1-3 μm vicinity of the devices to be planarized perfectly to the top devices. The hard-mask-assisted process also allows self-aligned via formation for metal interconnection to device top of μm size. The hard mask is then removed to expose a very clean device top surface for depositing metals for low ohmic contact resistance metal interconnection. The process is robust because it is insensitive to device height difference, spin-on polymer thickness variation, and polymer etch non-uniformity. We have demonstrated high yield fabrication of monolithically integrated optical switch arrays with mesa diodes and waveguide electroabsorption modulators on InP substrate with yield > 90%, high breakdown voltage of > 15 Volts, and low ohmic contact resistance of 10-20 Ω.

Keywords: Passivation, planarization, III-V semiconductor, optoelectronics, diode, integration, monolithic

1. INTRODUCTION

1.1. Background

To increase the functionality and performance of III-V semiconductor based devices while reducing their fabrication cost, one might take more and more monolithic integration approaches. That means one needs to integrate multiple and even different kinds of III-V devices from different III-V material growths and various process steps on a single substrate [1-3]. This is not a straightforward and easy task and many technologies have to be developed for robust and high yield processes that are still lacking in III-V semiconductor device monolithic integration. One of the requirement in III-V semiconductor devices is that they require passivation of their sidewalls after dry etching of the layered structures for the formation of the devices [4]. The passivation of sidewalls is needed to suppress leakage current between layers that may be operated at different bias and to increase device reliability as unpassivated sidewalls may degrade over time due to formation of conductive current path, such as that from oxidation of Indium in InP materials based III-V devices [5]. Another important aspect in III-V semiconductor devices is that they need low ohmic contact resistance for high speed operation, such as 10-100GHz high speed operations for optoelectronic devices and RF devices. To achieve low ohmic contact resistance, one would maximize contact areas by fully using device top area for metal interconnection using planarized structures. Thus planazriztion of the passivation materials to device top is another requirement in many of III-V semiconductor device process integrations. The challenge comes when device design is such that the top critical layers are only of sub-μm or even nm thickness and their sidewalls all need

*jun.f.zheng@Intel.com; phone 1 408 765-0920; fax 1 408 765-2387

passivation. A perfect planarization then must be needed so that the sidewalls of all the top layers are always sealed and thus passivated while at the same time the device top surface of the top layer is leveled with the surrounding passivation materials. The level of the planarization, defined by the step height between the device top surface and surface of the surrounding passivation materials, must be smaller than the thickness of the top layer, to assure that the interfaces between the top layer to be always sealed by the surrounding planarization materials.

Currently, passivation of III-V materials is conventionally accomplished by the use of polymer based materials such as BCB (bisbenzocyclobutane) that is spun on the wafer with pre-fabricated device structures [6]. The spin-on polymer layer is usually thicker than the devices in order to seal the device completely. Then planarization is achieved by etch-back of polymer to the device top to expose the top surface for metal interconnection [7]. Alternatively, one may need only to etch the polymer to certain level before reaching the device top and then use a mask and lithographic steps to form photoresist defined area for etching polymer to form an opening or via structure only to portion of the device top for metal interconnection [8].

1.2. Difficulties with current passivation and planarization methods

There are some difficulties with the conventional etch-back method. First of all, polymer etch-back method is limited to devices that are all of the same device height. When multiple growths of III-V layers happen on the wafer for different types of devices, the heights of all devices may be varied intentionally or unintentionally due to different growths, which makes it impossible for the polymer etch-back to land on all the device tops while at the same time to planarize all the device tops to the surrounding polymer. Secondly, even in the situation that we can have all the devices to be of the same height, and we can use *in-situ* etch depth monitor and automatic end-point etch stop control, we can only manage to etch stop at device top of a pre-selected location(s) on the wafer. The spin-on polymer thickness variation will make depth of polymer to be etched away change at different locations on the wafer. Polymer etch rate non-uniformity will demand the time required to etch the polymer away varies across the wafer. Thus, often one will end with wafers that has polymer over-etch or under-etch across the whole wafer in the etch-back planarization method. To assure etching to clear polymer from tops of all of the devices on the wafer, sufficient etch time is required to etch the polymer from a location requiring longest etch time. This will lead to many locations to have polymer over-etched and non-planarized where the step height between the device top and its surrounding polymer may be too large to be detrimental to the devices, e.g. leaving portion of the device sidewall un-passivated and resulting in devices to have high leakage current or even failure due to device breakdown. Even though we may design to have the device top layer thick enough to avoid the leakage or breakdown between layers, we still could suffer from metal step coverage issue if the over-etch induced step is too large. We can also encounter micro-loading induced micro-trenching due to over-etch at the interface of device and polymer. Such micro-trenching may lead to leaking current if the trench is deep enough to expose the sidewalls of critical layers and the micro-treching may lead to device shorting due to metal filling the micro-trench in metallization process. SEM image in Fig. 1 shows an example of such micro-trenching problem. Thus polymer etch back may not be a robust process.

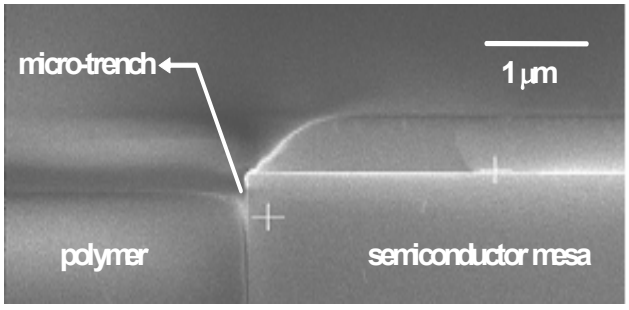

Fig. 1. A cross-sectional SEM (Scanning Electron Microscope) picture showing the formation of micro-trenching along the interface of the polymer and a semiconductor device after the polymer etch-back

Often there are polymer defects formed after polymer etch-back. Fig. 2 shows the void like defects from polymer surface after polymer etch-back. While the origin of such defects is beyond the scope of this paper, they may be attributed to the formation of voids such as bubbles during polymer spin or local polymer defects that would lead to enhanced local polymer faster etching. The existence of such defects, if present at the sidewall of a device, will lead to

an area of device sidewall that is not completely passivated, defeating the purpose of passivation and may leading to local leakage current. Thus the development of a method to prevent such defects at the vicinity of device and polymer interface will be very useful.

Another problem arising during polymer etch-back method is the some time incomplete removal of residual layer on top surfaces of the devices during polymer etch-back. The residual can be polymer itself or some contamination such as carbonized materials formed during the polymer etch or other processes. The removal of these undesirable residuals may be accomplished by polymer over-etch or oxygen descum process. However, polymer over-etch or oxygen descum process will also erode the polymer surrounding the devices, thus reducing the degree of planariziation and increasing the risk of micro-trenching as shown in Fig.1.

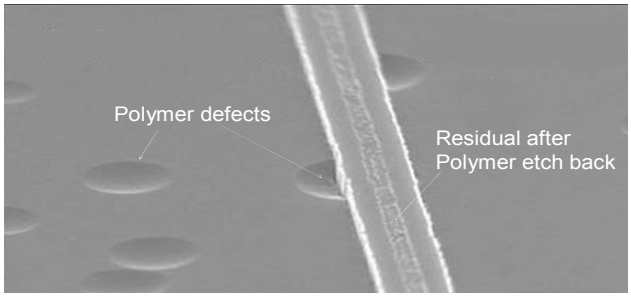

Fig. 2. A SEM top view image showing the formation of void like defects of ~ μm in size randomly distributed in the etched polymer surface. When such defects are located at the interface of polymer and device, there is a great chance that the defects will expose the device sidewall locally, leading to local unpassivated area.

The use of extra mask and lithographic steps to define selective polymer etch area for making path for metal interconnection to device top, or the via approach, may ease some problems such as the micro-trenching or polymer defects associated with polymer etch-back method, provided that the polymer opening is smaller than the device top. The via approach also avoids the need for perfect planarization and may works with devices that have different heights on a wafer. However, it has its drawback that it reduces the contact area on device top because the mask defined polymer etch area must be smaller than the device top to allow for mask alignment error and some degree of lateral polymer etch during the photoresist protected polymer etching process. While added cost is obviously undesirable in this via approach, the key problem is that it imposes a potential limitation to the device performance because it will increase ohmic contact resistance due to reduced contact area for metal interconnection. Such impact will be more significant at the device size of μm size or even nm size because the mask alignment error itself may take up sub-μm size.

In this paper, we introduce novel, wafer-level integration methods that address all the problems mentioned above in conventional polymer etch-back or via approach for planarization and passivation. We use a hard-mask-assisted planarization method that allows polymer to passivate the sidewalls all the way to the top of the layered devices across the wafer such that the polymer in the few μm vicinity of the devices is self-planarized to the device top with perfect flatness without a step, due to an undercut structure created in the hard-mask-assisted planarization process. Because of the perfect flatness, we can passivate and planarize advanced devices where the top layers may be only of sub-μm or nm thickness. Our method is applicable to devices with different heights, with spin-on polymer thickness variation, and with polymer etch non-uniformity. A variation of the hard mask assisted method leads to a self-aligning via formation process for smaller device of μm size where there is no room for undercut structure. Such self-aligned via formation process will use all the area of device top for low ohmic contact resistance metal interconnection, solving problem associated with conventional via approach.

We applied the new integration methods to fabricate an InP-based, optically-controlled optoelectronic switch arrays consisting of mesa PD (Photodiode) and a waveguide MQW (Multiple Quantum Well) EAM (Electroabsorption Modulator) integrated on the same substrate with diodes having different height [9-11]. We used BCB [8] as passivation polymer and we demonstrated functional integrated optical switches with high device yield of >90%, high breakdown voltages of >15V, and low ohmic contact resistances of 10-20 ohms, proving that this novel passivation and planarization process is robust.

2. METHODS AND RESULTS

2.1 Integrated process flows

Fig. 3 shows the basic process flow of the novel integration method. This process consists of: (a) defining the device area with the use of a hard mask; (b) dry etching or wet etching to form a device area; (c) retaining the hard mask while subsequently using selective wet etching in the lateral direction to create an undercut beneath the hard mask (a wet etch stop layer in vertical direction is needed in the device structure); (d) sealing and passivating the sidewalls of all device layers under the hard mask with a spin-on polymer, (e) curing the polymer and etching back the cured polymer passing the top level of the hard mask, and finally (f) removing the hard mask to create a passivation structure, with the polymer around the device perimeter completely leveled with the device top, i.e. a perfect planarization. Depending on where the polymer etch-back process is stopped with respect to the hard mask and the semiconductor device levels, various end polymer profiles might be obtained for different purposes with different advantages for III-V device integrations.

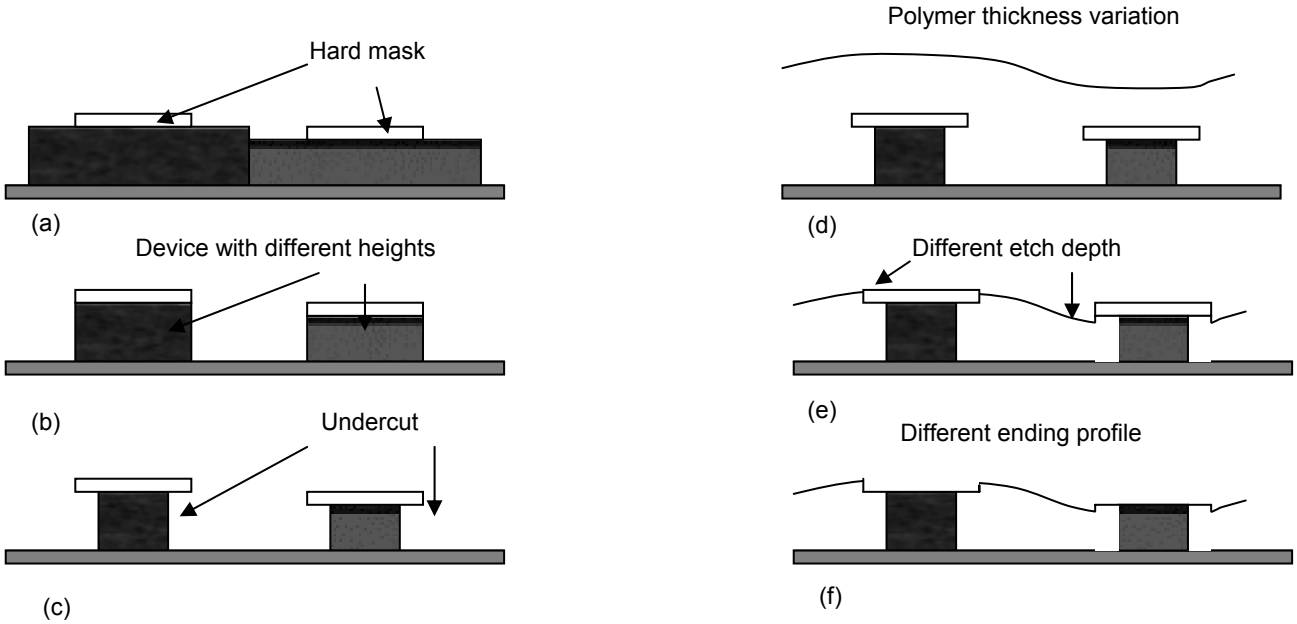

Fig. 3. Illustration of the self-aligned planarizing passivation process sequence: (a) Start with defining hard masks on the device wafer with epitaxial layers, which may consist of different selectively grown regions, (b) define device areas by vertical etching, (c) selectively remove the device material underlying the perimeters of the hard masks to create undercuts, (d) while retaining the hard masks, seal the device including sidewall under the masks using a spin-on polymer, (e) etch back the cured polymer passing the top levels of the hard masks, and (f) remove the hard masks to open the device top for metal interconnections.

As shown in Fig. 3, with the use of the undercut, this integration technique is robust and is insensitive to device height difference, spin-on polymer thickness variation, and polymer etch non-uniformity. The undercut structure also protects the polymer covered by the hard mask from etch-induced damages such as micro-trenching as shown in Fig. 1 and the formation of void like defects as show in Fig.2. The details will be discussed in sections 2.2 in this paper.

The most important feature shown in Fig. 3(f) are that the polymer at the vicinity of the device top is perfectly planarized to device top despite that we may have different ending polymer profiles: (1) When a hard mask is relatively thin, we only over etch the polymer to the level passing the bottom of the hard mask to assure that all the polymer above device top are removed. In that case, the device top, together with its hard mask and the polymer under hard mask, is a protrusion like structure above the overall etched polymer surface, as shown to the right of Fig. 3(f). This leads to a

quasi-planarization surface due to the steps created at the edge of hard mask, whether before or after the removal of the hard mask. Such steps should not impact the needed device passivation as they are away from the device sidewall and polymer interface. The only restriction is that the step height should be small enough to allow good metal coverage across the wafer during subsequent metal deposition. An over-etching of 0.5μm polymer is typically sufficient to assure the polymer above the hard masks is cleared. (2) When a hard mask is relatively thick, we may not end to over etch the polymer passing the bottom of the hard mask. Then the removal of a hard mask in this situation will result in a "via-like" structure while the polymer is still locally perfectly planarized to device top as shown to the left of Fig. 3 (f). The "via" depth can be as much as 0.5μm without causing issues for metal coverage during metal deposition. The possibility of using a thick mask in this situation will further increase the margin for where and when to stop polymer etch-back. Because both protrusion and "via like" structure may be allowed to co-exist as shown in Fig.3 (f), we can greatly increase the process control margin. A total of 1μm process margin may be obtained, more than sufficient for compensating process variation due to the spin-on polymer thickness and polymer etch non-uniformity in most process and will be very useful in applications where there are device height differences.

In some devices or process integration, an undercut structure may not be desired such as in the situation where the WG (waveguide) cross-section profile must be precisely controlled, where wet etch is not preferred or a vertical wet etch stop layer may not be easily implemented, and where the devices are of μm or even smaller in size so that there is no dimensional margin for creating an undercut structure. Thus we must develop a process that can be used to fully passivate devices without the need for an undercut structure. Using a very thick hard mask for a via formation is a solution. Fig. 4. (a), (b) and (c) depict the sequence of a process flow using a very thick hard mask for that purpose. The very thick hard mask is needed for sufficient margin to allow polymer etch-back to stop between the top surface and bottom level of the hard mask everywhere in the wafer.

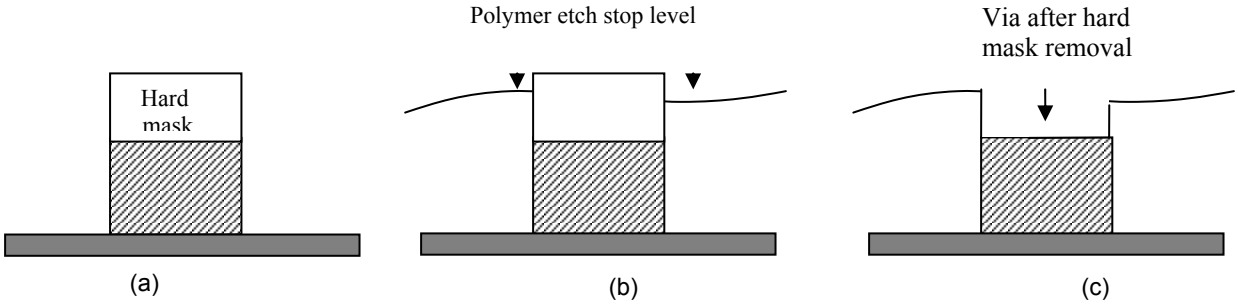

Fig. 4. Illustration of the self-aligned via formation passivation process sequence: (a) Start with hard masks with sufficient thickness on a device wafer with epitaxial layers and define device areas by vertical etch, (b) while retaining the hard mask, seal the device sidewall using a spin-on polymer and etch back the cured polymer stopping between top and bottom levels of the hard mask and , (c) remove the hard masks to form a via opening to device top for metal interconnections.

The hard-mask-assisted planarization approach with undercut configuration is especially suitable for devices with multiple heights, with large spin-on polymer thickness variation, and high polymer etch rate non-uniformity. The thick hard-mask-assisted via formation passivation method is very appropriate for small device feature where there is no room for creating undercut structures . Both integration schemes can be applied together in the same on-chip integration or they can be used separately basing on the needs. Together, they are very versatile integration techniques for much of the needed III-V passivation and planarization. With the spirit of sacrificial hard mask based process, we may further modify it in certain device structures to increase its utility, for example, using InP as sacrificial layer for deep via formation as discussed later in section 2.2.3. We will prove that the hard-mask-assisted passivation and planarizaion technique to be powerful for on-chip device integration, exemplified by the wavelength converter swicth arrays with dual diode configuration that we have made [9]. Details of the technique, directions this process can take, and results are discussed in the following sections.

In all the process integrations mentioned above, the hard mask is removed finally right before metalization, therefore a clean, polymer-free device surface is left for low ohmic contact resistance metal interconnection, which is another important advantage of these integration methods.

2.2. Process results

While the methods described above are applicable in III-V semiconductor device integration in general, we will discuss our process results in real device application in InP based III-V semiconductor devices.

2.2.1. The use of thin hard mask:

Applying the above integration methods, we first performed experiment with thin hard mask made of Si_3N_4 that is very commonly used in III-V semiconductor device processes. An circular device area of ~ 15μm in diameter is defined by Si_3N_4 hard mask. The wafer is then wet etched in 39% HCL (Hydrochloride acid) solution to form a mesa of ~ 3um in height. There is an extended undercut of 1-5μm around the perimeter of the InP mesa under Si_3N_4 hard mask, resulting an overhanging of Si_3N_4 hard mask over mesa like a "roof". It should be pointed out, that the final shape of the meas in this experiment is square instead of circular due to the HCL preferential etch of the InP along certain crystallographic orientations. A BCB is spun to form ~10μm thick BCB layer to seal completely the mesa and form a very flat top BCB surface. After BCB is cured at 250ºC for 2 hours, the BCB is etched back using a RIE etcher. The etching chemicals and etch conditions are such that the etch rate is 1.5-2.0μm/min and 0.1μm/min etch rate for BCB and Si_3N_4 respectively, resulting selectivity of more than 15:1 to assure Si_3N_4 is not etched away when there is BCB over-etch to be cleared from the Si_3N_4 hard mask. *In-situ* laser etch depth monitor was used for accurate control of the etch at wafer center. Right before etch depth reaches the top of the Si_3N_4, visual inspection of wafer will show that the colors over mesa area are changing indicating various remaining BCB thickness over Si_3N_4 hard mask. The etch is continued till we see color in all the mesa area to be blue color corresponding to the color of 0.1 μm Si_3N_4 hard mask. Then the wafer is dipped in 6:1 BOE (buffered oxide etcher) for 5min to remove the Si_3N_4. The removal of Si_3N_4 is clearly indicated by the change of the blue color to a typical white-gray color of underlying InP materials. Fig. 5 is an example of the color changes.

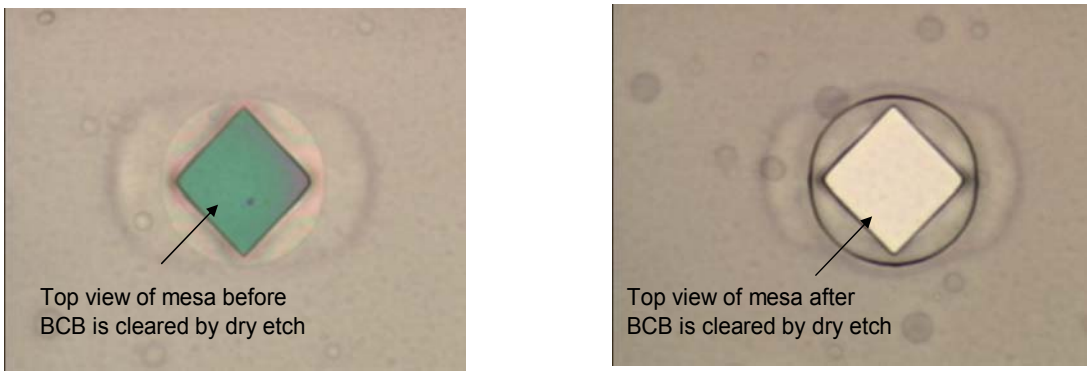

Fig. 5. (a) Optical micrograph image of polymer during etch-back process. (a) Before BCB is completely etched away on the top the Si_3N_4 hard mask.; (b) Image of the InP mesa and BCB surround the mesa after wet etching removal of the Si_3N_4 hard mask.

It is important to notice, that all the defects in the etched BCB, shown by colored circular shaped darker zones of μm in size, are outside the circular perimeter that the Si_3N_4 hard mask defines. We believe these are etch enhanced defects from BCB dry etching. Because of the "roofing" effect by Si_3N_4 hard mask for protection, area under the Si_3N_4 hard mask are free from of any of such defects. Obviously, we have no indication of trenching issues at the interface between the mesa and surrounding BCB, again due to the protection of the Si_3N_4 hard mask from dry etching. The details are more clearly indicated by the high resolution AFM images in Fig.6 (a) and (b).

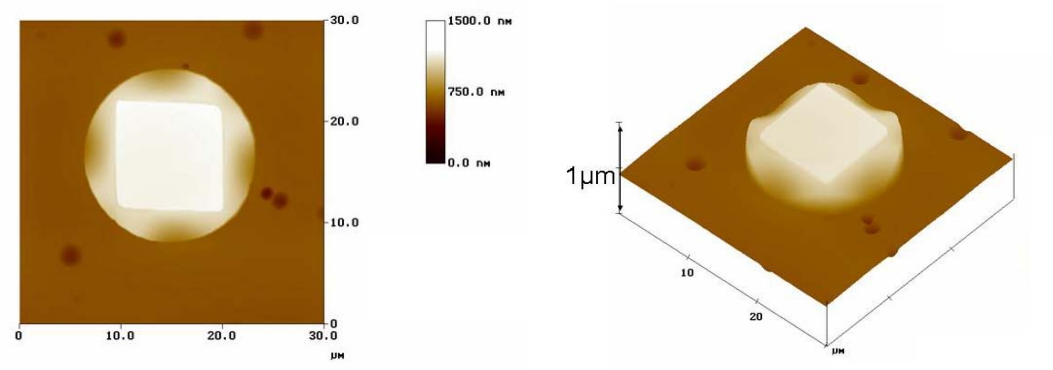

Fig. 6 AFM (Atomic Force Microscope) image of the meas and surrounding BCB: (a) Top view. The color indicates the depth of the etch surface. (b) 3D illustration of the same image. BCB under the hard mask is not etched and are about 0.5um above the etched BCB surface.

2.2.2. The use of thick hard mask

SiO_2 is more easily removed than Si_3N_4 by BOE. Another advantage of thick SiO_2 is that it will not impose too much film stress on wafer that is typically associated with the use of thick Si_3N_4. We can deposit thick SiO_2 to form thick SiO_2 hard mask that will allow BCB etch stop between the top and bottom levels of a thick SiO_2 mask. Upon removing of the hard mask, we can form a "via-alike" feature as discussed diction 2.1 Fig. 3(f).

We deposited 0.85um SiO_2 on InP device wafer for the formation of 0.85μm SiO_2 hard mask. Fig. 6 (a) is a top view and Fig. 6 (b) is a side view showing the SiO_2 hard mask remaining on the InP diode masa formed by wet etch using the SiO_2 as a hard mask. A desired ~2 μm undercut is uniformly distributed beneath the SiO_2 hard mask around the perimeter of the SiO_2 hard mask as shown in Fig. 6 (a). Fig. 6(b) is a cross-sectional SEM (scanning electron microscope) picture of the same mesa clearly showing the same undercut as reviewed from side. We then spun ~ 10um BCB and etch back it to expose the oxide hard mask in a similar way mentioned above for the thin hard mask case. The mesa with BCB etch-back to clear BCB above SiO_2 hard mask is shown in Fig. 7(a). After the oxide is finally removed by BOE (6:1) dip for 3-5min, we deposit metal overlay that is larger than the mesa to cover the whole area of the mesa

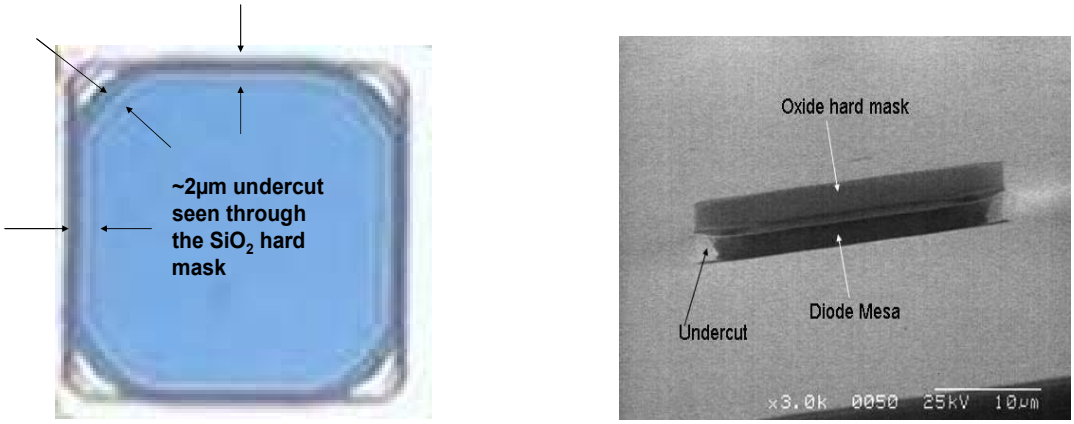

Fig. 6 (a) Optical top view image of a PD mesa and the oxide hard mask remaining over it. (b) SEM side view of the same mesa clearly showing that the oxide hard mask over the mesa with the 2μm wet etch undercut.

for low ohmic contact resistance metal interconnection, except that we leave the center portion open as optical window for optical beam to pass to the mesa diode. As you can see, the cross-sectional SEM in Fig. 7 (b) indicates that the top of the mesa and surrounding BCB under the metal overlay are perfectly leveled as we predicted basing on the integration method.

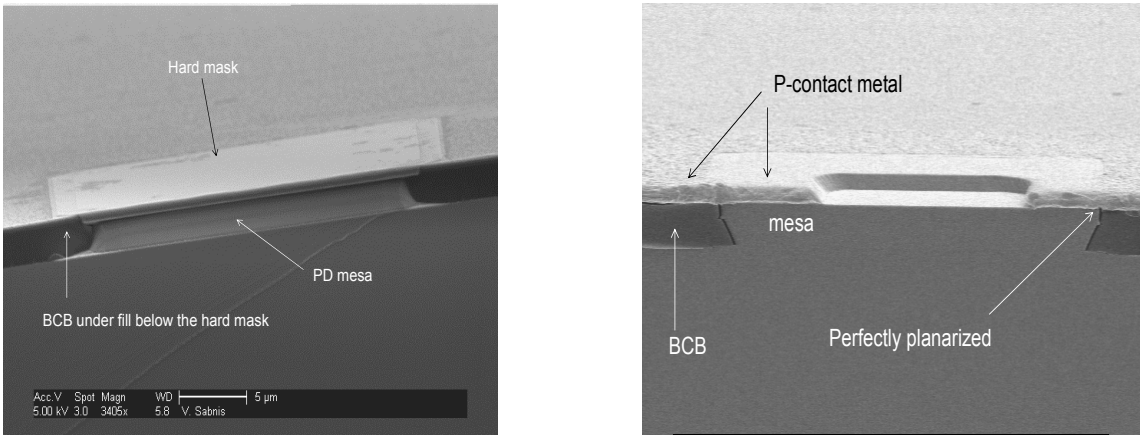

Fig 7 (a) SEM cross-sectional view of a PD mesa showing after BCB etch back to expose the SiO_2 hard mask for subsequent wet etch removal. (b) The PD mesa with top metallization.

To demonstrate that we have very clean surface upon the removal of oxide hard mask, we performed AFM image of the mesa top surface which was beneath the oxide mask. Fig. 8 (b) is an AFM image shows clearly all the atomic steps pertained from the MOCVD growth of InP based materials, indicating a very clean surface without any BCB residual.

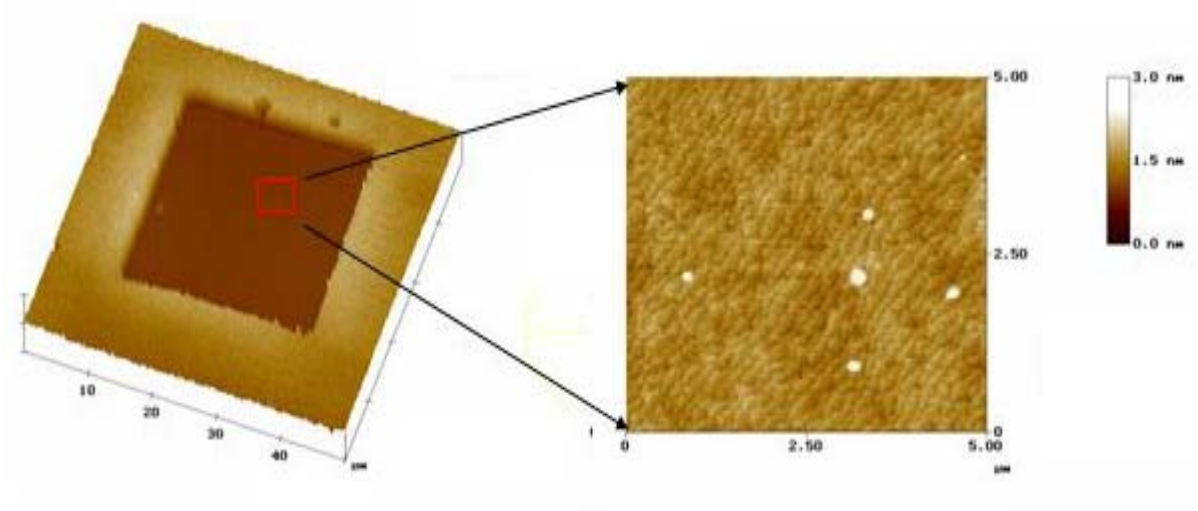

Fig. 8 (a) AFM image of an InP mesa with oxide hard mask removed. (b) An small area AFM image reveals only atomic steps from MOCVD growth of InP materials. Scattering white spot are paticles perhaps from wafer handling.

2.2.3. The formation of self-aligned via structures:

In addition to increasing the process margin in dealing with spin-on polymer thickness variation and etch rate non-uniformity, the methods mentioned so far also rely on the use of undercut structure for the protection of sidewall from micro-trenching and etch induced defects and for tolerating device height difference. As discussed before, the undercut structures are limited when we need to pasivate and planarize features of μm size such as WG MQW (Multiple-Quantum Wells) EAM (Electroabosorpton Modulators) because we have no room for etching induced undercut structures and wet etching for undercut may also destroy the WG cross-sectional shape undesirably.

However, we may simply use a very thick oxide mask to make the formation of a "via-like" structure as illustrated in Fig. 4 (a-c). Fig. 9 (a) below show an 0.75 μm thick oxide hard mask used for this purpose. Due to lack of the "roof" protection from hard mask with undercut structure, a 45º degree sloped oxide hard mask edge is purposely formed by wet etch formation of oxide hard mask to prevent the micro-trenching associated with polymer etch-back process. Such sloped structure is very effective as shown in Fig. 8(a) that there is no formation of microtrenching.

Upon the removal of the SiO_2 hard mask by BOE wet etching. A via-like shaped structure would be formed for metal interconnections. Such formation of via by the hard-mask-assisted process can be further extended to the use of InP as additional sacrificial layer for increased etch stop control margin in the self-aligned via formation process. The use of InP as additional sacrificial materials is possible because we can use the typical p-contact layer made by InGaAs as wet etch stop layer in the selective removal of InP. Fig. 9(b) is the result of the use of InP sacrificial layer as an addition to the use of oxide hard mask. The formed self-aligned via size is about 1 μm and we believe that we can further scale down the integration toward sub-μm size devices. The details will be published later.

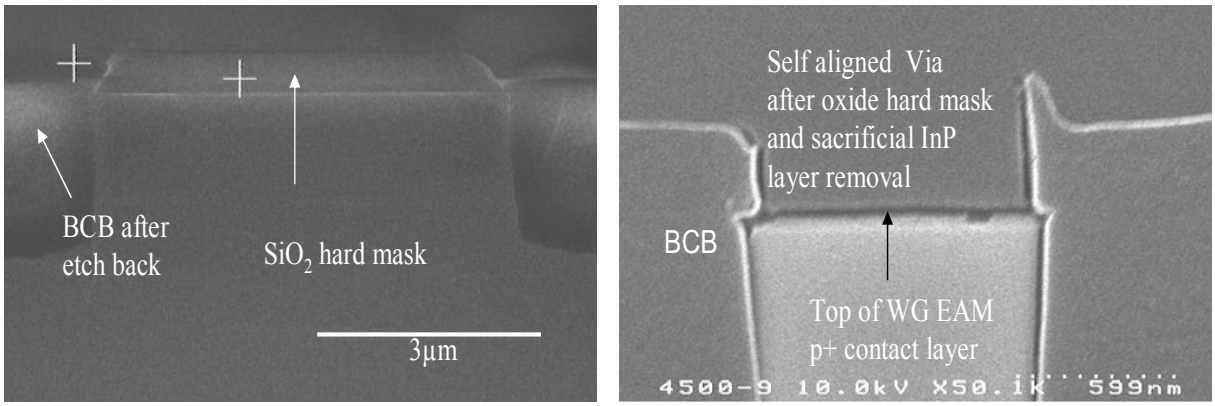

Fig. 9. (a) SEM cross-sectional image of the 5μm structure with the oxide hard mask retained after InP etch. The spin-on BCB was etch back and stopped in between the top and bottom of the oxide hard mask. (b) SEM cross-sectional image of smaller WG structure of ~1μm. InP sacrificial layer was served as an additional hard mask to increase etch-back depth control margin.

3. DISCUSSIONS

3.1 Applications of the methods

To further verify the developed methods, we have applied them to the fabrication of a dual-diode wavelength converter array device in which we have many mesa PD and WG MQW EAM intimately integrated in an arrayed configuration in one chip for cross-bar switch operations [9]. Due to different epitaxy growths, the PD and WG EAM exhibit device height difference of about 0.3-0.5μm, which make it very challenging to passivated and planarized such device by conventional polymer etch-back method. We have successfully made the high yield functional wavelength converter device arrays using some of the techniques discussed here.

First, we applied the thick oxide hard mask based method for the passivation and planarization for the formation of the PD as shown from Fig. 6 (a-d). We achieved > 90% diode yield on the integrated devices at wafer level. Diodes show IV characteristics indicating leakage of less than 1μA at 10V and breakdown voltage of > 25 Volts. The forward bias IV slope indicates that we have less than 10 Ohm contact resistance. This excellent low contact resistance value is consistent with the very clean surface after removing the oxide hard mask as shown in Fig. 8(b).

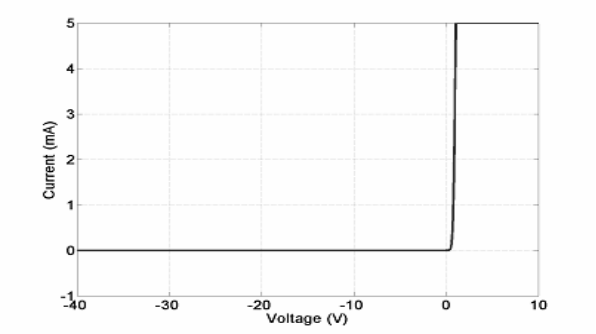

Fig. 10. A typical IV curve from the PD made by using the thick oxide hard-mask-assisted planarizing passivation method. The leakage at -10 Volts bias is smaller than 1μA

We fabricated WG MQW EAM with passivation and top layer metal interconnection formation using thick SiO_2 based via formation assisted by additional sacrificial InP layer to increase the polymer etch stop control margin. We have made WG MQW EAM diode that is 2 μm in width. From IV curve shown in Fig. 10, the leakage at -10 volts is only a few μA and break down voltage is about 15 Volts. The reason that the breakdown voltage for WG EAM diode is lower than that of PD diode is because the intrinsic region thickness is only 0.5μm for WG MQW EAM diode as compared with 1.25 μm for the PD. Forward bias IV slope indicates 15-20 Ohms contact resistance. This is higher than that of the PD because the top contact area of the WG EAM is smaller than that of PD.

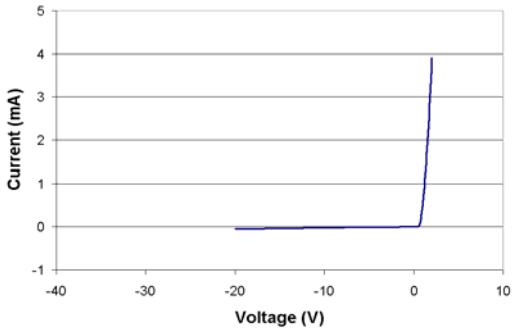

Fig. 10. A typical IV curves from the WG MWQ EAM diode. The passivation and top layer contact path is made by using the thick oxide hard mask and sacrifical InP layer assisted via formation process.

Finally, we fabricated integrated arrayed wavelength converter device on 2" InP wafers. The individual wavelength converter unit consists of intimately integrated PD and WG EAM. And the arrayed wavelength converter device is made from repeated units for aggregated cross-bar fabrics [9]. The wafer level passivation and planarization were accomplished applying the methods discussed above. The different PD and WG MQW EAM heights due to different growths [11], presenting a challenging test case for the developed planarization and passivation methods. It is critical for all the diodes in the arrays to yield so that a large nxm arrays will function. Applying the methods presented here in this paper, we have achieved 90% yield for all the diodes on the wafer, proving a robust planarization and passivation process. High yield for all the diode to function is critical for allowing larger size arrays to be made.

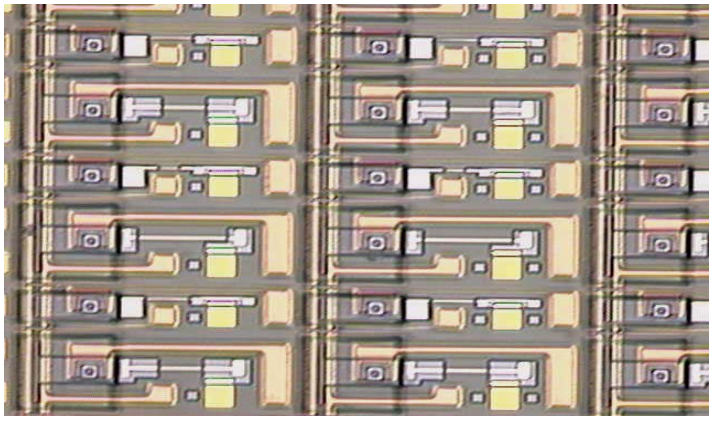

Fig. 11. Optical top view of part of an example arrayed wavelength converter device made on InP wafers. The top metallization is not formed yet, showing only the PD and WG EAM that are passivated and planarized with surrounding BCB.

4. CONCLUSION

The use of hard-mask-assisted passivation and planarization methods allow us to robustly fabricate monolithically integrated devices such as dual-diode optical switch arrays. These methods allow for passivation of the surface normal mesa diodes and WG diodes that may be different in heights by the self-aligned planarization process and via formation. The undercut structure in the process prevents etching induced defects at the device sidewall and surround passivation materials interface. The self-aligned via formation allows for maximun contact area for low ohmic contact reisitance metal interconnection to μm size device. The use of the hard mask that was already existing in the typical InP process is very benificial in that it keeps the device top very clean till the very last step when we are ready to remove it for final contact area metalization. The use of very thin or very thick hard mask is very varsatile allowing the process to be integrated with other requirements in a complex III-V integration. For future applications, the perfect planarization allows the device sidewall to be completely sealed and be further used for more advanced device design where the top critical layer may be of nm in thickness. The use of the hardmask and InP sacrifical layer allows self-aligned via formation at sub-μm size may be further extended into device that may be nm in size. The low leakage IV, high breakdown voltage, and high diode yield process prove that the methods presented here have potential for large scale monolithically integrated device fabrication.

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