# Evolution of the SEED Technology: Bistable Logic Gates to Optoelectronic Smart Pixels

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(*Invited Paper*)

***Abstract*—This paper reviews the recent evolution of quantum-well self-electrooptic effect devices (SEED's) for application in free-space optical switching and computing systems. Requirements of these systems have simulated, first, the development of devices usable in large systems of cascaded devices (the symmetric SEED), second, large two-dimensional arrays of these devices with improved physical performance, third, logically smarter extensions of these devices (logic-SEED's) and fourth, devices integrating electronic transistors with quantum-well modulators and detectors for both reducing the required optical energies and increasing functionality. We summarize this progress and its implications for future developments.**

## I. Introduction

For several years, researchers have been proposing the use of optics in information processing, computing, and telecommunications switching. These systems may be either digital, where the logic devices make some decision at each stage in the network, or analog. Some of the research on digital systems has concentrated on the use of two-dimensional (2-D) arrays of optical logic gates. In such experimental systems, optical inputs and outputs normal to the plane of the arrays are routed from one array to the next using optical components such as lenses, beam splitters, and even holographic optical elements. These systems are often called "free space" because the beams are unguided as they pass from one device array to the next, although in most cases the propagation is through both air and glass. One class of devices that has been used for many such system experiments is the quantum-well self-electrooptic-effect devices (SEED) [11], [12]. The evolution of the SEED has been very strongly influenced by the needs of system experiments, and some of the lessons learned here go beyond the specific SEED technology. In this paper, we will review the SEED's evolution, with emphasis on the more recent work that has been influenced more by systems than physics. We will also discuss primarily digital devices, although the technologies that we will discuss in the paper can be applied to analog devices as well.

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The SEED historically grew out of work on optical bistability [3], [4]. Much of the early work on bistability was motivated by the idea that optics could avoid some of the intrinsic speed limitations of electronic systems. With the demonstration of optical bistability in semiconductors, researchers felt that large, 2-D arrays of devices could be made. Parallelism, due to the large number of optical interconnections that could be made between devices from several of these arrays, became an increasingly important reason for interest in optics for processing. In proposed systems with many devices operated in parallel, however, the optical energy required to run the devices remained a major problem, so that the energy requirements, rather than the speed of an individual device, became the main limitation on the speed at which any system could run. Although optical devices could be envisaged that approached the logic energies of good electronic devices [5], to do so appeared to require very small devices in high-finesse resonant cavities. One approach was to make high-finesse microresonators and address the fabrication and optics problems that such devices have [6]. Another approach, taken by the SEED's, was to try to exploit fundamentally new physical mechanisms with very low operating energies. In doing so, however, the SEED abandoned the idea of an all-optical device. The SEED involves, internally, a change in voltage. This fact appears to discard the advantage of being able to make very fast devices by avoiding electronic processes. In fact, individual SEED's can be fast [7], and system speed is still limited by optical power for systems using arrays of devices. The fact that SEED's are not "all-optical" has been fortuitous, because it has also allowed this technology to advance first towards physically more sophisticated devices that are usable in digital systems and second towards the logically much "smarter" devices discussed in this paper.

The physical mechanism exploited by the SEED's is the quantum-confined Stark effect (QCSE) [8], which is an electroabsorption mechanism observed in quantum wells. Changes in voltage across the quantum-well layers can cause significant changes in optical absorption, either increases or decreases depending on wavelength. These changes can be large enough (e.g., a factor of 2 or 3) in a 1 $\mu$m thick multiple quantum-well stack to allow devices

to work with light beams perpendicular to the surface of a semiconductor wafer. Thus, one could imagine parallel optical interconnections between 2-D arrays of these devices. The energy required to make these absorption changes is a few $fJ/\mu m^2$, an energy density lower than that of most optical mechanisms for absorption change, and comparable to that of good electronic devices. Incidentally, SEED-like devices have also been proposed using bulk semiconductors [9]. However, the absorption change in bulk devices is generally much smaller than in devices using quantum wells.

The physics of the QCSE has been reviewed elsewhere [9], as have many of the different modulating and switching devices that can be made using it [10]. The history and physical processes of SEED's have also been reviewed [2], and so we need repeat little of the detail of this here. The essence of the SEED is that it combines one or more QCSE optical modulators with one or more photodetectors and some circuitry to give a device with optical inputs and optical outputs. Although such a device converts from optics to electronics and back again, it can be efficient and fast provided that it is integrated.

The circuits for the SEED can be very simple, the simplest consisting of only one quantum-well diode, a resistor, and a voltage supply (the resistor SEED or R-SEED) [1], with the quantum-well diode operating simultaneously as both detector and modulator. This circuit is optically bistable, and, like all of the other SEED's, needs no resonator for its operation (although these can be added if desired). The next more sophisticated from substituted another photodiode for the resistor (the diode SEED or D-SEED) [12]. This substitution allowed integrated devices to be made, leading to the first SEED arrays [11]. An important practical point about the SEED's is that many of the device types can be made in very large arrays with good yields, especially the symmetric SEED (S-SEED) that forms the basis for most of the devices discussed in this paper. The availability of arrays has been crucial in permitting systems experiments. One very useful physical point about these and most of the subsequent devices, is that they can be run either slowly at very low power levels or fast at higher power levels. The ability to run with little power makes systems experiments much easier, while still allowing the possibility of scaling up to higher speeds if sufficient power becomes available.

It is from this point on that systems experiments start to have a significant influence on SEED evolution. The next phase of this evolution was to come up with a device that met all of the physical requirements for devices in digital logic systems [13], [14]. The first attempts at systems tried to use arrays of D-SEED's. Although these were relatively uniform for simple bistable devices, these proved very difficult to work with because of the necessity of critical setting of thresholds for the devices (critical biasing) [15]. This is a classic problem of so-called "two-terminal" devices. The solution to this problem was the S-SEED (symmetric SEED) [16], which is a "three-terminal" device that does not have a critical biasing problem. The S-SEED, however, exploits the flexibility of a device that is internally electrical. It wires two quantum-well diodes together to give a device that is bistable in the ratio of two light beam powers, and is a circuit that has no counterpart in all-optical devices.

The S-SEED has been a very useful vehicle for systems experiments. Because the S-SEED does meet the necessary minimum physical criteria for a logic gate in a large digital system, several relatively large experiments have been conducted with it. These experiments have included an optical processor [17], and various generations of experimental photonic switching systems for telecommunications [18], [19]. Some of this work also drove the technology for making larger arrays of S-SEED's [20], [21].

The philosophy for the use of optics in digital machines has also advanced. There is considerable consensus now that many of the potential advantages of optics lie in its ability to communicate information. Optics has the physical potential to circumvent many of the limitations of electrical interconnections in large electronic systems [14]. These features of optics include: 1) no frequency-dependent loss or crosstalk; 2) essentially no distance-dependent loss or degradation in transmitted signals; 3) intrinsically very high bandwidth; 4) possiblity of large numbers of interconnections, without clock skew, in 2-D arrays; 5) possibility of global interconnect topologies, with many paths "crossing"; 6) electrical isolation; 7) immunity to electromagnetic interference; 8) the possibility of fundamentally lower communication energy (quantum impedance conversion) [22]. Free-space optics offers particularly radical possibilities of very large numbers of interconnections and global interconnection patterns. Many of the optical techniques and possibilities have been reviewed [23]. One particularly relevant point is the realization that electrical interconnections over short distances are good in integrated systems, with optics offering advantages mostly at longer distances (e.g. 100 $\mu$m or longer) [22], [24]. This gives a physical argument for "smart pixels"—locally smart, perhaps partly electronic, units that are optically connected externally.

The physical argument for smart pixels has also coincided with systems experience gained from the S-SEED processors and switches. Experiments on both of these classes of systems have suggested that the optimum partitioning of the system is not that of very simple logic gates globally interconnected, but rather asks for smarter "blocks" before the global interconnection. This gives an empirical argument from systems for "smart pixels". These realizations of the importance of smart pixels have also pushed the SEED evolution into a third phase, that of incorporating more logical functionality. This leads to the multistate SEED (M-SEED) [24], logic SEED (L-SEED) [25], and field-effect transistor SEED (F-SEED or FET-SEED) [26] discussed below. The issue of optical power requirements is still an important one for SEED's and the FET-SEED also attempts to reduce the optical energy requirement through the use of electronic gain.

The remainder of this paper is organized as follows. In

Section II, we briefly describe the behavior of the simpler optically bistable SEED's, and the evolution leading up to the S-SEED. The subsequent evolution of the S-SEED technology itself is discussed in Section III, including performance improvements and large arrays. The various logically more sophisticated devices based on the S-SEED technology are discussed in Section IV. Incorporation of transistors for energy reduction and greater logical complexity is discussed in Section V, and conclusions are drawn in Section VI.

## II. Early Approaches to SEED Optical Logic Gates

As mentioned above, the first SEED, the R-SEED, was a simple bistable circuit with a resistor, a quantum-well diode, and a voltage source [28] as shown in Fig. 1(a). In this device the p-i-n diode modulator also acts as the photodetector. The operation of the device can be described as follows. Suppose initially, no light is incident on the photodetector. Then since there is no current, essentially all of the power supply voltage appears across the photodiode, reverse biasing it. As we increase the optical input power, the photocurrent generated by absorption in the diode causes a voltage drop across the resistor, and the voltage across the photodiode decreases. If we operate the device at a wavelength where a decrease in voltage causes an increase in absorption, then this decrease in voltage causes an increase in photocurrent. This increase in photocurrent causes a larger voltage drop across the resistor, further reduction in voltage across the photodiode, further increase in absorption, and further increase in photocurrent. This will continue until the quantum efficiency of the photodiode drops off as it approaches forward bias (near 0 V) or until the forward current of the diode rises with forward bias. The net result is that the device switches abruptly from a high to a low voltage state. A similar argument can explain switching in the reverse direction. Since we assumed increasing absorption with decreasing voltage, this switching from "high" to "low" voltage state corresponds to the optical output being switched from a "high" to a "low" optical state. This switching concept is an example of bistability from increasing absorption [29], and many other examples are known.

Arrays of bistable SEED's were made that use photodiodes for the load instead of resistors as shown in Fig. 1(b) [12], [30]. In these diode-biased SEED's (D-SEED's), the bias and signal beams at 850 nm were incident on the quantum well p-i-n diode and a bias beam at 633 nm, for example, was absorbed in the load photodiode. The load photodiode could qualitatively be thought of as a resistor whose value was controlled by the 633 nm incident optical power. The use of the load photodiode instead of a fixed resistor made integration of the load easier, allowing demonstration of devices with performance that did scale well with decreasing device size and that was not dominated by stray capacitance. This was an important step, showing that integrated optoelectronic devices could have good switching energies. A second important point was that, unlike other bistable devices, the operating power was not fixed during fabrication. In fact, the operating range of the devices could be scaled by adjusting this optical bias to the photodiode over a range of over 7 decades in power. The use of the load photodiode also allowed new functions to be performed; the device could act as a dynamic memory, where the device could hold either of its two states for up to 30 s with both the red beam and infrared beams removed and could be used as a spatial light modulator [30]. Arrays as large as 6 × 6 were made [30].

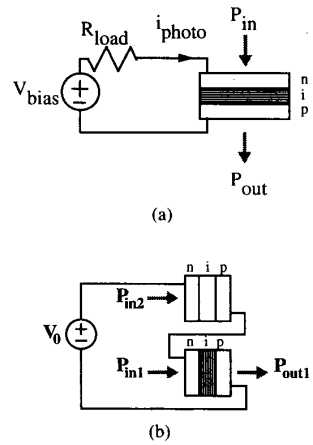



Fig. 1. Early SEED's: (a) Resistor biased and (b) photodiode biased SEED's.

Although the resistor biased SEED, and the integrated diode biased SEED in particular, offered the potential for major improvements in operating energies compared to most intrinsic bistable devices, the proposed operation of these devices in systems was similar to these traditional bistable devices. That operation included a bias beam to set the device just below threshold and an incident input signal to provide just enough energy to switch the device past its threshold. Provided the incident signal energy was small, optical gain could be achieved in that the difference in the *bias beam* output power from the device could be greater than the *signal* input power that was applied. One problem with using this approach to implement, for example, a NOR gate was that if the bias beam was too large, the device might inadvertently switch with 2 logic "zero" inputs, and if the bias beam was too small, the device would require too large a signal to switch for the case of a logic "one" and a logic "zero" input, and thus have insufficient gain [15], [31], [32]. Thus, the bias beam power needed to be controlled quite tightly, and several researchers believed the variations in optical power of an array of bias beams would be too great to permit operation of a large 2-D array of logic gates. Futhermore, the device could be easily switched by any reflections back into the output of the device, because the device makes no distinction between the input and the output "ports". These problems of "critical biasing" and poor input/output iso-

lation are classic issues with so-called "two-terminal" devices. Thus, researchers believed the answer was a "three terminal"device, analogous to the transistor in electronics, that would achieve the required optical gain, but would not require precise control of the optical bias beam, and would not amplify any reflections back into the output.

Several devices showed promise for satisfying this requirement. The first of these was the optical logic etalon (OLE) [6], that used a traditional GaAs Fabry–Perot etalon device but operated with two pulsed beams, each at a different wavelength. The input or pump beams were absorbed by the etalon and shifted the position of the Fabry–Perot peak if they had sufficient intensity, as would be the case for a logic "one" input. Subsequently, the probe beam was either transmitted or reflected by the etalon, depending on whether the position of the Fabry–Perot peak was shifted, which in turn depended on the logical state of the input beams. The transmitted probe beam was the output. Because the input and output beams had different wavelengths, a pair of complementary devices were needed, one to up-convert and one to down-convert. A device that absorbed at a wavelength longer than the unabsorbed probe beam was never successfully made, although with a strong isolated absorption peak one could in theory do this.

A group of proposals, which could be collectively called transistor biased SEED's (T-SEED's), are also three terminal devices [33]–[40]. An example T-SEED is illustrated in Fig. 2. In these devices the input light is incident on a phototransistor. The output of the phototransistor is then connected in series with a quantum-well modulator. Because of the current gain in the phototransistor, the signal beam could be weaker than the bias beam incident on the modulator. Thus a weaker signal controlled a stronger one. Both hybrid devices and integrated T-SEED's have now been demonstrated.

One surprising aspect of the T-SEED is that the use of the transistor in these simple circuits does not greatly reduce the optical energy required at the input of the device; hence we can make little use of the transistor gain to improve system speed. The reason for this is the so-called "Miller capacitance" effect, well known from vacuum tube and transistor amplifier. Essentially, the input photocurrent has to generate all of the charge that is involved in changing the voltage across the base-collector capacitance, with no help from the transistor current gain [2]. The current gain is useful only for charging stray capacitance and the modulator capacitance. Bipolar transistors can also be difficult to scale to small dimensions because surface recombination can reduce current gain. An additional issue with bipolar transistors is that it is difficult to predict and control the precise current gain. This means that, in a system, we cannot rely on any specific value, and it is likely to vary from transistor to transistor. Hence we need schemes that could take advantage of the gian without requiring a specific value. One such scheme is to use pairs of transistors in a differential configuration, with

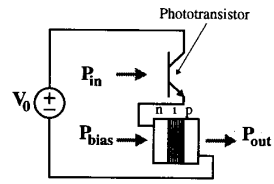


Fig. 2. Transistor biased SEED.

pairs of input light beams and pairs of output light beams [29]. Such differential devices could be made, and might be usable in systems, but since these T-SEED's offer little optical energy advantage and may require pairs of beams anyway, the S-SEED, with its simple diode structure, has been used instead for many systems experiments. The major additional requirement for the use of the S-SEED is that the optical power supply beams need to be clocked. This is not a major disadvantage for a digital system since clocking is needed anyway. There are, of course, several interesting ways in which transistors can be used to reduce optical input energy requirements and improve logical functionality, but these generally require more sophisticated circuits that can easily be implemented in a purely vertical integration. We will discuss some of these later below.

The S-SEED [16] is a simple device that does have all of the necessary attributes, such as "three-terminal" behavior. It operates in a relatively unusual way, but, because it does satisfy all of the requirements for use in digital logic systems, it has proved relatively easy to perform quite complex systems experiments with it. The S-SEED is still optically bistable, but it is bistable in the ratio of two beams. The S-SEED shown in Fig. 3 has two p-i-n diodes, each containing quantum wells in the intrinsic region, with one diode behaving as the load for the other and vice versa. Because the switching of the device depends on the ratio of the two optical inputs, the S-SEED is insensitive to optical power supply fluctuations if both beams are derived from the same source. The device has time-sequential gain, in that the state of the device can be set with low power beams and read out with subsequent high power beams. The device also shows good input–output isolation, because the large output does not coincide in time with the application of the input signals. Therefore, the device does not require the critical biasing that is common to most optically bistable devices, and has the attributes of a three terminal device.

In operation, two sets of two beams are incident on the device. First, a pair of unequal power beams (signal beams) sets the state of the device. Provided the difference in power between the signal beams is sufficiently large, we can force the device to be in one of two possible states. A contrast ratio of 2 : 1 is more than sufficient to ensure this, and since the signal beams will likely be derived from the output of another S-SEED, the contrast ratio will normally be greater than 2 : 1. This is illustrated in Fig. 4(a) and (b). In these figures, the photocurrent versus voltage for each of the diodes is plotted as a func-

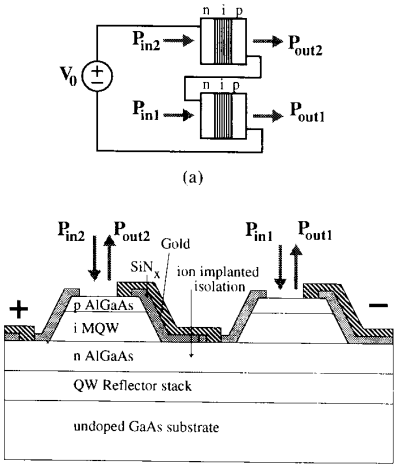



Fig. 3. Symmetric SEED (a) schematic diagram and (b) layer structure [20].

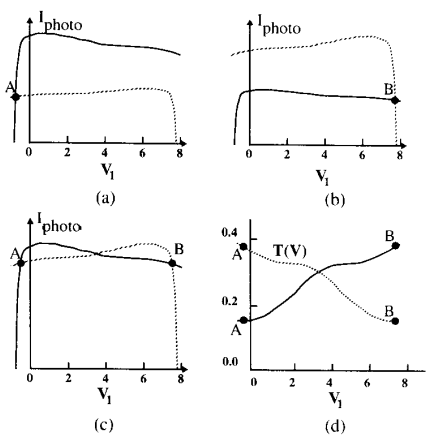



Fig. 4. Photocurrent (a)–(c) for both diodes of an S-SEED versus voltage across the bottom diode. Solid lines are for the bottom diode and dashed lines are for the top diode. (a) Optical power into the bottom diode is twice that of the top diode. (b) Optical power into the top diode is twice that of the bottom diode. (c) Optical power into the two diodes are equal as is the case when the clock beams are applied. (d) Measured reflectivity for both diodes of a reflection mode S-SEED versus voltage across the bottom diode. Again, solid lines are for the bottom diode and dashed lines are for the top diode.

tion of the voltage on the bottom diode [i.e., $V_1$ in Fig. 3(a)]. In Fig. 4(a), the incident optical power into the bottom diode is twice that of the top diode, and the device is in state A corresponding to low voltage across the bottom diode. In Fig. 4(b), the incident optical power into the top diode is twice that of the bottom diode, and the device is in state B where the voltage across the bottom diode is approximately equal to the supply voltage. These figures also illustrate that the ratio of input optical powers determines the state of the device and any common variations in the optical powers of the two signal beams will scale both photocurrent curves together and not result in a change of state.

The second set of beams are equal-power clock beams that are used to read the state of the device. During the application of the signal beams, the clock beam powers must be low compared to the signal beam powers. After the state of the device has been set, we apply the equal power clock beams to each diode to read the state. In Fig. 4(c), the photocurrent versus voltage is plotted for each of the diodes as a function of the voltage on the bottom diode with equal light power into both diodes. For equal powers, the device can be in either of two stable states shown by points A and B in Fig. 4(c). (The center intersection point is unstable.) Which one of the two states the device will be in depends on the state of the device before the clock beams were applied. In Fig. 4(d), we show the optical input/output characteristics for each of the two quantum-well diodes as a function of the voltage across the bottom diode. For state A, the upper diode has a higher output power than the lower diode (for equal input power clock beams), and for state B, the lower diode has a higher output power than the upper diode. Because the device when read is nominally operated in the center of the bistable region and the bistable loop width is wide, there are rather loose requirements on the equality of the clock beams.

The state of the device is independent of the common clock power and only dependent on the state of the device before the clocks were applied. Therefore, the input clock powers may be many times greater than the input signal powers that were used to set the state of the device, and the device has optical gain. It is not optical gain in the sense of an optical amplifier where the optical signal itself is amplified, but, in this device, the weaker signal beams control a set of stronger clock beams, much like in a bipolar transistor where a weaker base current controls a stronger collector current. Because we apply the signal beams first and then the block beams, we refer to this as "time-sequential gain". In addition, because the output does not coincide in time with the application of the input, the device has effective input–oputput isolation in that a reflection of the output signal back onto the input will not occur at a time when the device is most sensitive to the input. Because of the internal capacitance of the device, it can hold its state (i.e., the voltage on the two diodes) for a short period of time without any incident light. Thus, it does not matter is there is a time when no light is present between the removal of the signal beams and the application of the clock beams. Therefore, the timing of the optical inputs is not critical.

Since bistability is typically observed over several decades in optical powers [41], we can have a large effective signal gain. Of course, switching at low powers takes proportionately longer, so that gain is obtained at the expense of switching speed. Thus, the device has a constant gain–bandwidth product. The amount of gain needed in a system built entirely with S-SEED's will be determined by the absorption losses in the devices themselves, the fan-out of the devices, and reflections, absorption, and scattering losses in the optical components used to intercon-

nect the devices. We want to minimize these losses so that the signal beams will be as large as possible and the switching time will be small.

The switching time of the S-SEED is determined by several factors, and the switching times of all SEED's without transistors are similar to that of the S-SEED. First, the response time of the semiconductor quantum-well material to an applied electric field is very fast, in the range of a few hundred femtoseconds [42]. As detectors, the electron and hole escape times from the quantum wells vary from roughly 1 ns to less than 10 ps [43]–[46], depending on the quantum-well structure and the applied electric field. The device also has an *RC* time constant due to the series resistance of the metallic leads and the diode and parasitic capacitances. For the arrays of devices that we will describe in the next section, the *RC* time constant is also ~10 ps [7]. By using mode-locked pulses to deliver the power to the device rapidly, switching times for S-SEED's have been measured as low as 33 ps [7].

The switching time in a system is limited by the time it takes the photocurrent to charge and discharge the diode and parasitic capacitances. This time is approximately proportional to the input optical power, the area of the device, the change in applied electric field accompanying a change in state, and inversely proportional to the device responsivity [47]. The required optical switching energy can be defined as the amount of optical energy incident on one window of an S-SEED that causes the device to change states and this energy is approximately equal to the switching time times the optical input power. Required optical switching energies of ~1 pJ are typical for devices with 5 $\mu$m × 10 $\mu$m optical windows operating at ~6 V bias. For a device with a required optical energy of 1 pJ, an input optical power of ~1 $\mu$W, would give a switching time of 1 $\mu$s, and an input optical power of 1 mW would give a switching time of 1 ns.

We can summarize the many desirable characteristics of the S-SEED for performing optical switching and processing experiments: 1) large arrays of devices can be made with uniform characteristics; 2) they operate with low energies so that single mode semiconductor laser diodes can be used to operate many (up to 2048 cascaded [48]) devices at once, although at low speeds; 3) the operating power range of the devices is very large, from less than 1 nW to greater than 100 $\mu$W; 4) the devices have differential inputs and outputs so that common variations in signal powers are less important; 5) the devices can have high gains, greater than 10 000, without critical biasing and the actual gain is dependent on clock and signal powers rather than being predetermined; 6) the devices operate at dc so that visual inspection can determine if an array of devices is operating correctly; 7) the devices have high input–output isolation, because the outputs and inputs do not coincide in time; 8) the devices perform signal logic level and timing restoration at each stage; 9) since a new clock beam is generated at each stage in a multistage network, optical aberrations do not accumulate; 10) they are reversed biased devices which are robust and require small currents and low voltages to operate; 11) the devices can operate as a logic gates, static or dynamic memories, and simple switching nodes; and 12) they can operate over several nanometers in wavelength and the dc bias may be increased to increase the operating range. These features have enabled several system demonstrations to be built using S-SEED's [17]–[19] that would have been difficult or impossible with devices without many of these characteristics.

Recently, "dynamic" operation of the S-SEED's has been demonstrated [49]. In dynamic operation a single input beam (or two beams for NOR operation) is incident on one of the two diodes of the S-SEED's (the "write" diode). Assume, for the moment, that the device is in an initial state with essentially the supply voltage across the "write"diode. If the input signals have sufficient energy (a logic "one") they will change the state of the device, otherwise (two logic "zeros") it will remain in its initial state. Then, a high power mode-locked beam incident on the other diode (the "read" diode) reads its state. The pulse width of the mode-locked beam must be shorter than the sweep out time of the diodes, otherwise it will change its state before reading. After the state is read and the carriers are swept out of the intrinsic region of the diode, the state of the device will be reset, by the photocurrent generated by the read beam, to its initial state.

Operation in this mode is similar to the OLE device, and one could use diodes that are sensitive at different wavelengths to make a two wavelength S-SEED [50] comparable to the two wavelength OLE. Dynamic operation has some disadvantages compared to "conventional" S-SEED operation; these include the necessity of using mode-locked pulses, the fact that energies need to be controlled more precisely, and better contrast ratios are required to allow for nonuniformities of the optical system for an array of devices. The main advantage of this dynamic operation is that the required optical energies per beam and the number of beams are reduced. It is interesting to note, again, that one needed the flexibility of an optoelectronic device to realize this type of logic gate, and that it could not easily be made using an "all-optical" nonlinearity.

## III. S-SEED Technological Evaluation

The first S-SEED's consisted of 2 × 1 arrays of transmissive mode devices [51]. The mesa sizes were 200 × 200 $\mu$m with 100 $\mu$m × 200 $\mu$m optical windows. Optical energies were ~320 pJ and the fastest switching time measured was ~40 ns. The next generation of devices had many improvements [20]. They were made in a manner referred to as "batch fabrication" in which whole wafers of devices are processed at a time using techniques found on GaAs *IC* production lines. These devices had integral dielectric mirrors grown as part of the layer structure as shown in Fig. 3(b). These devices, often referred to as reflection mode devices [52], have several advantages over transmission mode devices. These are: 1) the

optical signals pass through the quantum well region twice, thus increasing the contrast ratio; 2) the substrate does not need to be etched from the back of the devices, thereby making fabrication easier; 3) signals are incident from a single side only, simplifying mounting of the device and allowing a single imaging lens to image light beams onto and off of the optical windows; 4) the device array can be mounted directly to a heat sink. Heat removal is important, not only because of reliability, but also because a change in temperature will cause the wavelength of the excitonic peak in absorption to shift.

Initially, four different devices sizes were made with mesa sizes ranging from $(100\ \mu m)^2$ to $13.5\ \mu m \times 14.0\ \mu m$ with corresponding optical window sizes from $40\ \mu m \times 80\ \mu m$ to $5\ \mu m \times 10\ \mu m$. The required optical energies scaled with mesa size as expected from 150 pJ to 3.5 pJ at 15 V (7 fJ/$\mu$m) [53], although a slight increase in optical energy density was observed for the smallest of the devices. Switching times of less than 1 ns were measured by using mode locked pulses to set and reset the state of device. Photocurrents and reflectivities for a $16 \times 8$ array of devices were uniform to within $\sim \pm 10\%$, and all of the devices were working in roughly 50% of the $16 \times 8$ device arrays. A subsequent mask set had $16 \times 8$ arrays of smaller devices with $2.5\ \mu m \times 4.0\ \mu m$ mesas [54] and $64 \times 32$ arrays of S-SEED's with $10\ \mu m \times 10\ \mu m$ mesas and $5\ \mu m \times 10\ \mu m$ optical windows [21], with a further reduction in required optical energies to 2.5 pJ at 15 V.

Although the required optical switching energies scaled with device area, the excitonic peak in photocurrent at low applied voltages was reduced in the small devices. As a result of this, the larger devices exhibited bistable characteristics at 2–3 V yet the smaller devices required 10 V for bistability. It was determined that recombination of carriers at the mesa sidewalls caused this reduced photocurrent [55]. In the small mesas the proximity of the mesa sidewalls to the photogenerated carriers caused recombination to occur before the carriers had time to escape from the wells. For the large devices, the carriers could escape from the wells and be swept out of the intrinsic region because the carriers were not near the sidewalls.

One solution was to redesign the quantum well structure so that carrier escape times would decrease, lessening the effect of surface recombination. As a consequence of the reduced carrier escape times, saturation intensities should increase, allowing device operation at higher optical powers. Modulators with different barrier widths and heights were made and the saturation intensities measured [43]. It was found that reducing the barrier width from 60 to 35 Å improved the saturation intensities by a factor of three. A further improvement of a factor of three or so was found in devices with 60 Å barriers with 20% aluminum instead of the usual 30%. Electron escape times were measured and the escape times of the 35 Å devices were much faster than the 60 Å barrier devices, especially at low fields [43]. There is some understanding of the underlying physics, with thermionic emission and tunneling, both resonant and nonresonant, all contributing to the carrier escape times [44]. Little or no degradation in the electroabsorption of the devices was observed with the lower or thinner barriers. Recent experiments have also confirmed that the hole escape times can also be short in such structures [46].

As a result of these measurements, arrays of S-SEED's were made with the barriers reduced from 60 to 35 Å. The smaller devices exhibited a strong excitonic peak in the photocurrent. Thus, the required voltage for bistability was reduced from 10 V in the 60 Å barrier devices to 2–3 V in the 35 Å barrier devices for mesa sizes of 13.5 $\mu m \times 14\ \mu m$ [7] and $10\ \mu m \times 10\ \mu m$ [56]. Additionally, the switching speed of the devices improved from $\sim 1$ ns to $\sim 33$ ps as measured using mode-locked pulses to set and reset the devices [7]. In addition to improved barrier designs, recent S-SEED arrays with as many as 32768 elements ($256 \times 128$) have been made and electrically addressed S-SEED's have been made in $16 \times 8$ arrays [57]. Integrated $8 \times 8$ arrays of S-SEED's have also been made with a diode clamping circuit maintaining moderate electric fields across both diodes of the S-SEED's at all times [58]. These "diode-clamped" S-SEED's operated with a voltage swing of only 2 V, and a required optical energy of only 340 fJ.

Other quantum-well structures have been designed that have given further improved performance. One of these designs has barriers with only $\sim 2\%$ aluminum [59]. Surprisingly, strong excitonic peaks in the absorption spectra are observed for low applied fields, although there is no excitonic peak for applied fields greater than a few volts per micrometer. While this can be detrimental in some applications, for a S-SEED, where a large change in absorption is desired for a small change in electric field, the change in absorption for these ultrashallow barrier devices can be larger than for a conventional barrier design. It was also found that the total carrier transit time was equal to that of bulk GaAs p-i-n diode detectors, which indicates that the transit time across the intrinisic region is longer than the escape time from the wells [45]. As a result of these fast escape times, the photocurrent peak in the absorption can occur at applied voltages less than zero, that is, the peak occurs in forward bias at voltages less than the built in voltage $V_{bi}$. Because of this, a self-biased S-SEED has been made [60] that shows bistability without a power supply.

A self-biased S-SEED has also been made using large area mesa diodes with asymmetric coupled wells [61]. The principle of the asymmetric coupled wells is that, with lower fields on the device, the electron and hole are likely to be in the wider of the two wells, and thus there will be a strong excitonic peak in the absorption. When an electric field of a few volts per micrometer is applied, the electron will be shifted to the narrow well and the hole will remain in the wide well. Thus, the absorption is reduced. The asymmetry between the well widths is used partly to compensate for the electron and hole separation induced by the built-in field of the diode. Both the shallow

barrier and coupled well S-SEED's were made using relatively large area mesa diodes. However, since the voltage swing in both of these devices is on the order of $2V/\mu m$, the required optical energies should be comparable to the diode-clamped S-SEED's for integrated small area devices.

Arrays of self-biased S-SEED's could be made without power supply leads. Such devices could be more densely packed and they should have higher yields because if one of the devices was short circuited, it would not short-circuit a whole array. It should be possible to define the array size after fabrication, because there are no common leads between elements. Self-biased devices should also have greater immunity to crosstalk and electromagnetic interference because of the absence of inductive coupling through the power supply leads.

Another improvement to SEED's has come from the use of a Fabry–Perot cavity to improve their contrast ratio [62]–[71]. In these devices, instead of applying an antireflection coating to the surface of the device, one could epitaxially grow a dielectric mirror on the surface (similar to the one on the bottom of the devices) or allow the reflection of the device–air interface occur at the surface. It is possible to design a device so that this reflection will "cancel" the reflection from the back mirror. Such a device would have zero reflectivity at one applied voltage and a finite reflectivity at another applied voltage. For this to occur, the reflectivities of the front and back mirrors should be different. Because of this, these devices are often called asymmetric Fabry–Perot modulators (AFPM's).

We can subdivide asymmetric Fabry–Perot modulators into two subclasses. Those that have low reflectivity with no applied voltage are said to be normally off and those that have low reflectivity with an applied voltage are normally on. Normally off devices will have decreasing absorption with increasing voltage and thus they are suitable for S-SEED's. Normally on devices are suitable as modulators or nonbistable SEED's. Contrast ratios greater than 100 : 1 can be achieved in the laboratory on actual devices [65]. However, it may be difficult to design and fabricate many arrays of devices with that contrast ratio *at a particular wavelength*, because of the stringent requirements that this places on epitaxial growth accuracy and uniformity. Although S-SEED's have been demonstrated using AFPM's [72], [73], because of the difficulties in making devices that operate at a particular wavelength and because systems using differential signals do not need devices with high contrast ratios, batch fabricated AFPM SEED's have not yet been used in systems requiring large arrays.

## IV. Extensions of S-SEED Device Concepts

Because of the success in building systems with the S-SEED's, and the desire to have greater local functionality, other devices with greater functionality were explored that had many of the same features as the S-SEED. One group of devices was the multistate SEED's (M-SEED's) [25]. Voltage biased M-SEED's consist of n diodes connected in series with a voltage source. With equal powers on each diode, there are n possible stable states. In each stable state, one of the diodes is in reverse bias and the other diodes are in forward bias. The particular diode in reverse bias will be the one that has (or had if all beams are currently approximately equal) the least optical power, provided that power was small enough to force the device outside of the multistable region. A device with three such diodes acts as an enabled S-SEED where a "high" signal on the third diode allows normal S-SEED operation of the remaining two diodes and a "low" signal on the third diode sets both outputs of the remaining two diodes (the S-SEED) to "low" optical outputs. This operation is analogous to tri-state electronic devices that have two active states (normal S-SEED operation) and one inactive or high impedance state (corresponding to the two "low" outputs). A simple switching node can be made using these tristate SEED's [74].

The M-SEED also has various interesting analog modes, including a "loser take all" circuit and image thresholding and other digital modes as well, including a device with $2^n$ stable states. None of these other modes has so far been explored for system applications. However, the understanding obtained from the M-SEED's has led to a class of devices whose application to optical processing systems is more apparent. This class of devices is known as Logic SEED's (L-SEED's).

In L-SEED's with the appropriate electrical connections of several quantum-well diodes, we can achieve nearly arbitrary logical functionality [26]. An L-SEED consists of a group of input diodes with incident input signals and a pair of output diodes (i.e., a S-SEED) that modulates a pair of equal power clock beams to provide the output is shown in Fig. 5. We have been most interested in differential L-SEED's in which a pair of beams represents the logic state of the inputs, although devices whose logic state is represented by the power levels of a single beam can also be made. For differential L-SEED's, the topology of the electrical connections between input diodes is identical to that of CMOS circuits. To obtain the required L-SEED layout, the n-channel devices in a CMOS circuit are replaced by diodes with incident uncomplemented signal inputs and the p-channel devices in the CMOS circuit are replaced by diodes that have complemented inputs.

As an example, consider a differential L-SEED to implement the function $E = AB + CD$ as shown in Fig. 6. This function can alternately be implemented by two S-SEED AND gates folowed by a S-SEED OR gate, but to do so would require two optical stages to perform the function that can be performed in a single stage with L-SEED's. The function $E = AB + CD$ implements a $2 \times 1$ switching node if $A$ and $C$ are the two data input channels and $B$ and $D$ are the two control channels. It can also implement the exclusive OR function of $X$ and $Y$ if $A$

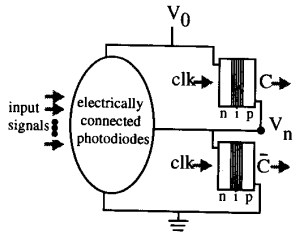



Fig. 5. Logic SEED schematic diagram. For differential devices, the topology of the electrical connections between diodes is identical to that of CMOS circuits.

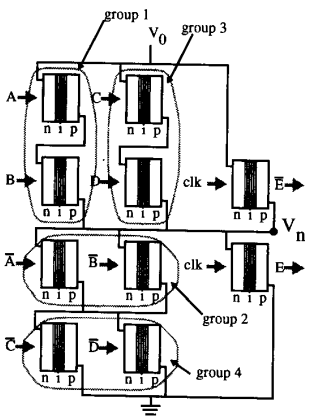



Fig. 6. Logic SEED implementing the function $E = AB + CD$. For a photonic switching node, $A$ and $C$ are data inputs, $B$ and $D$ are control inputs, amd $E$ is the output.

$= X$, $B = \overline{Y}$, $C = \overline{X}$, $D = Y$. For a switching node, if control input $B$ is a logic "1"and control input $D$ is a logic "0", then output $E$ is equal to data input $A$. Likewise, if control input $B$ is a logic "0" and control input $D$ is a logic "1" then output $E$ is equal to data input $C$.

Operation starts when the input signals are applied. The photocurrents generated in these input diodes sets the output node voltage $V_n$. Subsequently, a pair of higher power clock beams are applied to the output S-SEED to read the state. This operation achieves the same time sequential gain mechanism found in the S-SEED and performs retiming, logic level restoration, and wavefront quality restoration.

We can assume that a diode with a "high" incident optical signal will electrically go into forward bias and can be thought of as a "short circuit" across its electrical terminals. A diode with a "low" incident optical signal will remain in reverse bias and can be thought of as an "open circuit". We define an input to be a logic "one" when the uncomplemented input is greater than the complemented input (e.g., $A > \overline{A}$), and a logic "zero" is the reverse case. If inputs $A$ and $B$ are logic "ones", inputs $\overline{A}$ and $\overline{B}$ must be logic "zeros" because the data are complementary. Thus, group 1 will be short circuited and group 2 will be open circuited. Therefore, $V_n$ will be equal to $\sim V_0$ and, when the clock beams are applied, $E$ will be "high". Similarly, if inputs $C$ and $D$ are logic "ones", group 3 will be short circuited and group 4 will be open circuited. Therefore, $V_n$ will also be equal to $\sim V_0$ and, when the clock beams are applied, $E$ will be "high". However, if $A$ or $B$ is a logic "zero" and $C$ or $D$ is a logic "zero", groups 1 and 3 will be open circuited and subgroups 2 and 4 will be short circuited. Therefore, $V_n$ will also be equal to $\sim 0$ and, when the clock beams are applied, $E$ will be "low".

The L-SEED concept can be extended to devices that contain optoelectronic transmission gates. These optoelectronic transmission gates consist of two back-to-back photodiodes and perform the function of a transmission gate in CMOS circuits. Like their electronic counterparts, these devices electrically transfer the logic state from one device to another under external control, but in these devices the control is optical.

To make a $2 \times 1$ photonic switching node, three S-SEED's and two of these optoelectronic transmission gates are connected as shown in Fig. 7. In operation, first we apply the data inputs, $A$, $\overline{A}$, $C$, and $\overline{C}$ and the control inputs, $B$ and $D$, to the switching node and subsequently apply the clock beams clk which are modulated by $S2$ to give the output data $E$ and $\overline{E}$. Control inputs $B$ and $D$ are complementary. If control input $B$ is greater than control input $D$ (i.e., $B = 1$ and $D = 0$), then $V_2$ will be equal to $V_1$ and output $E$ will be equal to data input $A$. However, if control input $B$ is less than control input $D$ (i.e., $B = 0$ and $D = 1$), then $V_2$ will be equal to $V_3$ and output $E$ will be equal to data input $C$.

An optoelectronic shift register can be made using optoelectronic transmission gates as shown in Fig. 8. First, the input signals set the state of the S-SEED $S1$. Next, the clock beams clk1 and transfer beams Trn1 are applied simultaneously. The clock beams provide an optical output signal from $S1$ and hold the state of $S1$ while transfer beams Trn1 transfer the state electrically to $S2$. Then, clock beams clk2 and transfer beams Trn2 are applied to S-SEED $S2$ and transmission gate $T2$ to read the state of $S2$ and transfer the voltage on $S2$ to $S3$. Simultaneously, the input signals are applied setting the new state of $S1$. Analogous to electronic shift registers, the odd numbered S-SEED's are called master flip-flops and the even numbered S-SEED's are called slave flip-flops. Because of the two-cycle nature of the clock beams, a pair of S-SEED's (a master–slave flip-flop) holds one bit of information. Thus, $2N$ S-SEED's implement a $N$ bit shift register.

Several 2-D arrays of L-SEED's have been made using the same batch fabrication process as the S-SEED's [75]. A $16 \times 16$ array of L-SEED's that act as logic gates without the use of a preset beam has been made and individual NOR gates have been demonstrated using devices from this array. A $4 \times 4$ array of $E = AB + CD$ gates (Fig. 6) has been made and the functions of the exclusive OR gate and photonic switching node have been demonstrated using devices from that array. Perhaps the most interesting array is a $32 \times 16$ array of S-SEED's in which neighboring devices are connected with optoelectronic transmission

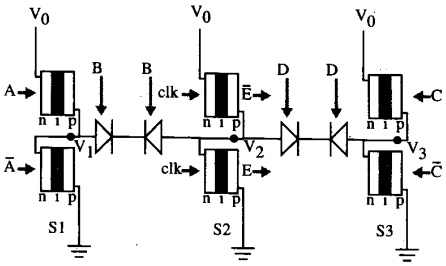



Fig. 7. Logic SEED 2 × 1 switching node using optoelectronic transmission gates $A$ and $C$ are data inputs, $B$ and $D$ are control inputs, and $E$ is the output.

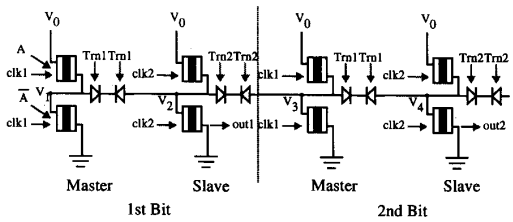



Fig. 8. Logic SEED optoelectronic shift register. $A$ and $\bar{A}$ comprise the differential input to the shift register, clk1, clk2, trn1, and trn2 are the clock and transfer beams, out1 and out2 are the parallel outputs ($\overline{\text{out1}}$ and $\overline{\text{out2}}$ are not shown but they are located above out1 and out2 in the figure).

gates. In this array, individual switching nodes, multiplexers, and demultiplexers have been demonstrated, an eight bit shift register has been demonstrated, and a 16 × 8 array of 2 × 1 switching nodes has been operated concurrently.

One way of understanding the L-SEED operation is to think of a quantum well photodiode (or any photodiode for that matter) as a three terminal optoelectronic device. This is illustrated in Fig. 9 where the photocurrent versus voltage across the diode is plotted at different input optical powers. If we ignore the shape of the photocurrent versus voltage curve, which is a consequence of the diode having quantum wells, the $I$–$V$ characteristics of the photodiode are similar to the $I$–$V$ characteristics of a field effect transistor except that the input optical power, instead of the gate to source voltage, controls the current. Complementary MOS circuits have complementary transistors. Since there are no complementary diodes, the equivalent function is performed by using a complementary input. Incidentally, the input diodes of the L-SEED's do not need to have quantum wells, although the analysis from the M-SEED principle shows that quantum-well diodes can be used. The ability to use quantum-well diodes for all diodes greatly simplifies fabrication, so all integrated L-SEED's have been in this way. Quantum-well diodes are, of course, essential at the output.

We can also envision devices in which there are optical interconnections between diodes as well as electrical connections between diodes. In this case, the quantum-well modulator/detector can be thought of as having three ports, an electrical port, an optical input port and an optical output port. A circuit model describing the characteristics of the device as shown in Fig. 10. One can then use circuit simulation programs to connect up devices both electrically and optically in arbitrary manner to realize functions that are difficult to calculate analytically.

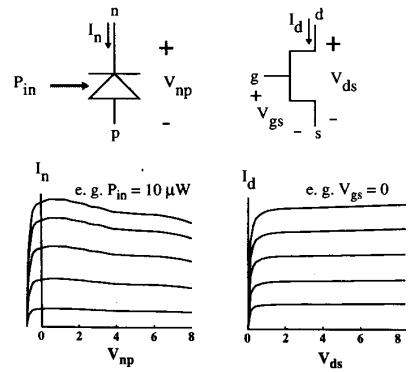
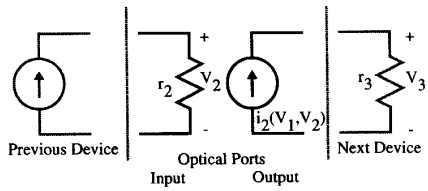



Fig. 9. A quantum-well photodiode as a optoelectronic transistor. (a) Current voltage ($I$–$V$) characteristics as a function of input power (curves were actually measured at one power and scaled accordingly) (b) ($I$–$V$) characteristics for a field effect transistor for comparison.

The S-SEED and L-SEED's are just two of many potentially useful "devices"' that one can envision using only quantum-well diodes. The point is that a quantum well diode technology exists and optoelectronic circuits can be designed in much the same way as electronic circuits are designed, with the added flexibility of providing both optical as well as electrical connections. If clever designs are used, these circuits will have the desirable features of the L-SEED's and S-SEED's that make them easy to use for optical signal processing experiments. The desire for a three terminal optical transistor has been replaced by the quantum-well modulator/detector that enables optoelectronic circuits of complex functionality to be designed.

## V. Transistor-Diode SEED Technology

A transistor-diode SEED technology offers advantages compared to a diode-only technology. These include the following: 1) Electronic cascading. The optical output(s) from one L-SEED logic gate can of course optically drive other L-SEED gates. While the electrical output from one L-SEED gate can be sometimes be used to change the electrical output of a second gate by using optoelectronic gate to the next for a wide variety of logic gates. 2) Electronic voltage gain can be provided in the circuit. If designed properly, the optical inputs would not need to provide as much charge (because the change in electric field at the input is less) as that needed by a SEED without electronic gain. By reducing the charge required, the optical energy that must be supplied by the optical input is reduced. 3) Electronic transistors can provide electrical isolation between input photodiodes, further reducing the capacitance that needs to be charged, and thus the optical energy required. 4) The optical inputs can be buffered by a single electronic gain stage which can then be used to provide local fan-out. In some cases this avoids having to



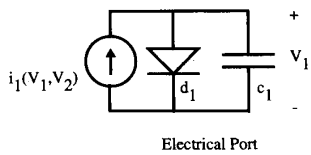




Fig. 10. Circuit model for a quantum-well modulator/detector. For the electrical port, $c_1$ is the diode capacitance, $i_1(V_1, V_2)$ is the photocurrent, and $V_1$ is the diode voltage. $V_2$ is an "artificial" voltage that represents the input optical power, and $i_2(V_1, V_2)$ is an "artificial" current that represents the transmitted (or reflected for a reflection mode device) optical power. By adjusting $r_2$ or by adding other resistors, one can take into account the optical losses between devices.

perform fan-outs optically. 5) Bistability is not required in transistor-diode SEED's. This allows one to use "normally on" modulators operating at a wavelength longer than the excitonic peak at zero field. These modulators generally have less loss in the "high" output state, and have less problems with absorption saturation compared to modulators designed to operate with the exciton peak at low fields [49]. 6) Because the voltage on the input quantum-well detector diodes is only varying by a small amount, the detectors can be biased for high responsivity during the entire switching transition. In addition, it may be possible to build transistor-diode SEED's with different detector and modulator structures, thus optimizing the detectors and modulators independently for the functions that they are performing. 7) Transistors can be made smaller than we can expect to make optical diodes. Thus, the transistor-diode smart pixel can have greater complexity for a given amount of area than a comparable L-SEED. The size of the present SEED's is not limited by lithography, but is limited by the current optical systems that image the arrays of spots onto the devices. The current SEED arrays have optical window sizes of $\sim 5\ \mu m \times 5\ \mu m$. While this size is relatively large compared to the smallest transistors, it is, however, small compared to the area of a bonding pad used to electrically interconnect integrated circuits. It is also much smaller than the relatively large output transistors used to drive electrical signals off of electrically interconnected integrated circuits.

There are several transistor-diode technologies that one might consider. One of these is to integrate GaAs field effect transistors with quantum well modulators and detectors. One such integration scheme is shown in Fig. 11 [26]. In this device, the quantum well p-i-n diode is grown with the p-type material on the bottom of the quantum-well region. The field effect transistor is made using the top n-type layer. In the first FET-SEED demonstration,

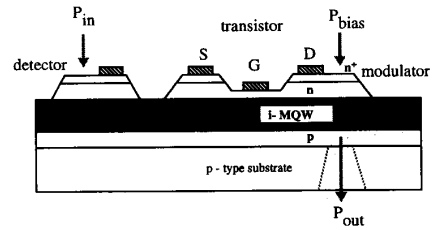



Fig. 11. Field effect transistor SEED (FET-SEED) layer structure [26].

the top n-type layer was GaAs [27]. Thus a standard MESFET could be made on top of this material. Subsequent batch fabricated FET-SEED's incorporated several improvements [76]. One of these was that the top n-region contained a heavily doped GaAs channel and an undoped AlGaAs layer. In either of these approaches, the absorption of the incident light is small in the FET layer. The batch fabricated devices also contained integral dielectric mirrors and gained the advantages of having reflection mode devices. A third improvement is that the bottom p-type layer could be made insulating between devices using ion implantation, so that arbitrary connections between diodes and transistors were possible. Early circuits show that the individual circuit elements (transistors, resistors, quantum-well diodes) work as expected [77], and recent measurements have confirmed that devices can be made with optical energies below 100 fJ [76].

Another potential transistor-diode technology is to integrate GaAs heterojunction bipolar transistors (HBT's) with quantum-well modulators. One particularly attractive approach is to integrate the quantum-well region in the base-collector junction of the HBT as shown in Fig. 12 [78], [79], [36]. The advantage of this approach is that only a single device is made. By contacting the bottom n- and p-layers, one has a quantum-well modulator/detector. By contacting all three layers, one has an electrical HBT. One can in principle make a heterojunction phototransistor by contacting the top and bottom layers, although the turn-off time of phototransistors will be too slow because of the Miller capacitance of the device. (The Miller capacitance problem can, in principle, be avoided by separating the input and output stages and designing for little or no voltage gain in the first stage. This generally requires lateral integration because of the need for several transistors, and this is possible with this integration scheme.) In the early devices, the quantum-well region inhibited current flow through the collector base junction. By using ultrashallow barriers in the quantum-well region, a device with improved transistor characteristics has been made [79].

Transistor-diode SEED smart pixel circuits may have two forms. The first is that the pixel contains a number of receivers, electronic logic, and a number of output modulator drivers as illustrated in Fig. 13. The purpose of the receiver is to provide the optical to electrical conversion and to provide electronic gain so that less optical power is needed to generate the logic level signals. It is not clear

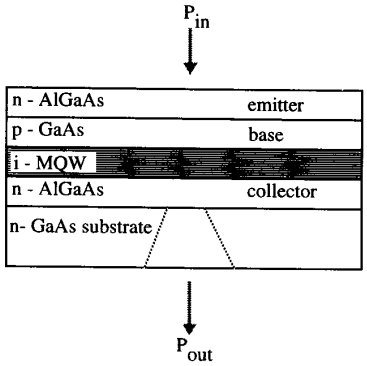



Fig. 12. Heterojunction bipolar transistor-SEED layer structure [76].

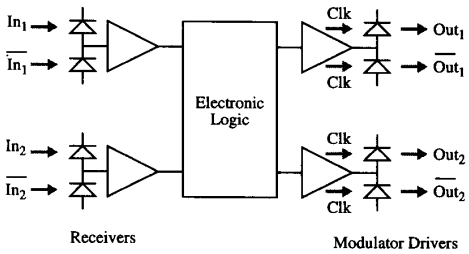



Fig. 13. Generic smart pixel consisting of one or more receivers, electronic logic, and one or more optical modulator drivers.

what the best form of a receiver would be, and it is quite difficult to design one that has all of the attributes of the symmetric SEED. For the ultimate application of smart pixels for at least one thousand interconnections, an ideal receiver would have the following characteristics: 1) low power consumption; 2) low delay variations, which in practice means low overall delay, and thus few gain stages; 3) low voltage gain (threshold variations, rather than thermal noise, will limit the sensitivity of the inputs); 4) few power supply leads; 5) dc coupled so that arbitrary data patterns (e.g., a long string of "ones" or "zeros") may be used; 6) high transimpedance (a 1 V output for 10$\mu$A input means $Z_t$ = 100 K; 7) large dynamic range to be operable at low or high powers and have good tolerance to power level variations; 8) operation at low and high bit rates so that visual verification of device operation is possible; 9) tolerance to electrical noise and crosstalk on the power supply leads; 10) while high sensitivity is desired, smart pixel receivers will likely have low sensitivity compared to communications receivers, because of the need for dc coupling, low delay, and circuit simplicity. For example a required optical energy of 23 fJ is equal to $10^5$ photons. That 23 fJ is almost two orders of magnitude lower than our current S-SEED's (with 5 $\mu$m $\times$ 10 $\mu$m optical windows), yet it is two orders of magnitude *higher* than a good communications receiver with a sensitivity of 1000 photons/bit.

The logic family ideally would have complementary devices to minimize power consumption and allow the utmost in design flexibility. Of the GaAs FET technologies,

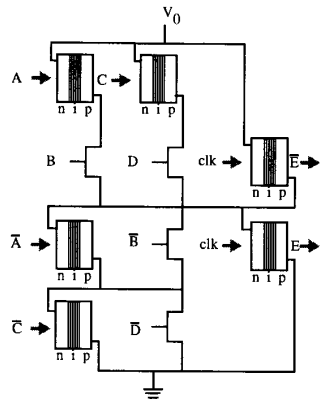



Fig. 14. Transistor-diode implementation of a 2 $\times$ 1 switching node with electronic control, (*B* and *D*), but without separate receivers for each data input (*A* and *C*).

direct coupled FET logic (DCFL) has traditionally had the lowest power consumption and smallest transistor count.

The purpose of the output modulator driver is to amplify the signal from the logic to the higher voltages required by the quantum-well modulators. DCFL typically has voltage swings of $\sim$0.6 V which is too small to drive the quantum-well modulators. The modulators typically require from 2 V (ultrashallow barriers [59]) to 5–6 V [2].

A second variety of smart pixels is to combine optoelectronic transistors (quantum-well modulators and detectors) with electronic transistors. An example of such a circuit is shown in the 2 $\times$ 1 switching node in Fig. 14. We have already seen in Fig. 6, a L-SEED 2 $\times$ 1 switching node with all optical inputs. For many applications, the control of the node may need to be electrical. By simply replacing half of the input quantum well diodes in the L-SEED by transistors, we can have electrical control. Although this particular circuit may not be the optimal way to implement this function, there is more flexibility in designing circuits when one can mix and match optoelectronic and electronic circuit elements arbitrarily, as opposed to the circuits that are of the form of Fig. 13. While the required optical input energy will be greater than if all of the optical inputs are amplified, the hardware savings (in terms of the number of transistors) can be substantial. It might seem from this discussion that we are simply moving backwards from optical devices toward electronic ones again. However, the real power here is to be able to mix the two arbitrarily to take advantage of the best features of both to benefit the system overall. This is the aim of the transistor diode SEED technologies.

## VI. Conclusion

We have discussed the evolution of the self electro-optic effect devices from the early bistable logic gates to a developed diode SEED technology as well as early experiments in transistor-diode technologies. We have

focused primarily on enhanced functionality as the devices have evolved. As improvements in quantum well modulators are demonstrated, these improvements are incorporated into the SEED technologies. We gave the example of the improved barrier design; additional enhancements such as manufacturable Fabry–Perot devices with high contrast ratios and arrays of devices that operate at solid state laser wavelengths, such as 1.064 $\mu$m, are likely to be incorporated into the SEED technologies. Perhaps the most compelling improvement that will be coming in the next few years is that the electronic gain associated with transistor-diode technologies may enable demonstration systems to be built at data rates exceeding 100 Mb/s. While it will be more difficult to establish a high yield batch fabrication process for a transistor-diode technology, many of the applications of these technologies will require large scale integration, and thus the establishment of this technology is going to be necessary for the future success of optoelectronic processing systems.

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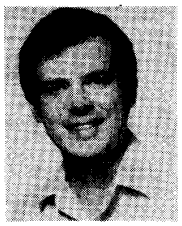

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