Digital Optics

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Digital optics is a technology for processing, transport, and storage of optical digital information. Digital optics offers both the high temporal bandwidth as in fiber communications as well as the high connectivity and information density of optical imaging. The energy dissipation per bit of communicated information, as well as the chip area dedicated to interconnections, can be significantly lower in optics than in high-speed electronics. This motivates the introduction of parallel optical interconnections through free space in communication-intensive areas of digital information processing such as switching in telecommunications and within multiprocessors. Digital optical circuits can be constructed by cascading two-dimensional planar arrays of optical logic gates interconnected in free space. The state of the art and the trends in digital optical information processing systems are reviewed for optical logic, optoelectronic interfaces, and optical free-space interconnection systems.

I. Introduction

A. Synopsis

The increasing demand for speed and throughput in digital information processing systems suggests the need for novel technologies in addition to microelectronics. The future impact of optics on data processing is described here in a top-down approach. First, the concept of "digital optics" is introduced as it emerged from past theoretical and experimental work on optical computing. Second, the superior interconnection abilities of optics are compared with microelectronics. Finally, the key technologies for digital optical information processing are discussed: optical interconnects introduce design constraints conceptually different from those of electronic interconnects. Consequently, systems design must be adapted to optics. Optoelectronic components are needed as interfaces between microelectronics and optics as well as for data regeneration and for logic functions. All-optical logic gates are currently in the research state. Laser systems are needed as optical power supplies to provide logic devices with light. Optical systems based on imaging need to be built for implementing regular interconnections, data permutations, and systems for data splitting and joining. Any useful data processing system will be fairly complex. Therefore problems related to manufacturing and packaging need to be addressed. Since there are so many technologies involved (computer science, semiconductor physics and processing, laser physics and classical optics), we cannot dwell too heavily on any one technical detail. Rather, we attempt to give an overview picture of the interdisciplinary research in the field of digital optics.

In this paper we focus on one specific approach: computing with array interconnections through free space. Other approaches have been promoted and a comprehensive comparison will be necessary in the future. We believe that free space optics will become competitive with electronics within the next few years in some pilot applications such as self-routing switching networks in telecommunications. Applications in the field of supercomputing will follow later.

B. The Roots of Digital Optics

The earliest root, which is around 40 years old, is the field of optical analog information processing. Some of the highlights of optical analog processing were spatial filtering and holography. Van der Lugt performed matched filtering for the purpose of pattern recognition. Cutrona and his coworkers decoded optically the raw data obtained by side-looking radar. The appropriate spatial filters were produced at first by photographic methods, later on as holograms. Lohmann introduced computer-generated holograms to increase the processing flexibility. Analog processing was useful for digital optics for two reasons.

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First, it introduced "information thinking" into the community of physical optics; concepts like spatial frequency and space-bandwidth product illustrate the educational effect upon the optics community. Second, as a lasting contribution from optical analog processing, is the set of hardware tools, like matched filters and computer holograms.

The step from analog to digital has been attempted twice before the current "third phase of digital optics," which began around 1980. The first phase was triggered by the invention of the laser in 1960. Then optical logic gates based on laser quenching were proposed. At the end of the first phase it was concluded [1] that optical logic is not a viable technology for thermal reasons. The second phase, around 1970, was concerned with architectural concepts like residue arithmetics, but no competitive nonlinear devices or logic gates were available. A brief account of the two earlier phases did appear elsewhere [2]. The third phase was triggered by the discovery of nonlinear optical effects in semiconductors. Optical bistability [3], optical logic gates, and optically controlled modulators of light beams were invented with performance data comparable to electronic devices.

As the minimum feature size in VLSI is reduced and the complexity on-chip is increased, the overall processing speed is limited by interchip and interboard communications. Attempts are being made to use many processors in parallel to get around this speed problem. This, however, further increases the need for efficient interconnection systems, since all the processors have to communicate. Three-dimensional optics has been proposed for interconnecting VLSI systems [4]. Imaging systems offer, besides parallelism and high data rates, the possibility to implement global communication networks such as the perfect shuffle [2]. In the field of microoptics, new approaches similar to stacked planar optics [5] are emerging and are useful for packaging hybrid optoelectronic processing systems.

In the last few years an increasing effort has been devoted to computer architectures specifically tailored to optics [6]. More details on various approaches to optical computing can be found in a special issue of the IEEE PROCEEDINGS on optical computing [7], in a lead article of IEEE SPECTRUM [8] (among other things a waveguide-based architecture for supercomputers), and in a special issue of *Applied Optics* on optical computing [9].

C. What is Digital Optics?

Digital optics comprises techniques for data processing, for short- and long-distance data transport, and for short- and long-term information storage. Today, long-distance optical digital data communication through fibers is an established technology. Long-term optical mass storage is coming into general use. For data processing, however, the optical signals still need to be converted to electronic signals which are processed electronically. A uniform technology for digital optical information processing, comparable in its significance to microelectronics, does not yet exist and is by itself a challenging research goal.

Digital optics requires several key components that are currently in different stages of development. System design and architecture must be adapted to optics. Two-dimensional optoelectronic and optooptical, switching devices, or logic gate arrays, exist in their first generations. They are comparable in their performance to electronic switches. Modules for parallel interconnections through free space, data splitting and combining, and devices for beam shaping are currently in development.

II. DIGITAL OPTICAL INTERCONNECTIONS

One general argument for the use of optics is that it is good at communicating information. Optical fibers are now the preferred method for telecommunications and very high bit rates can be handled without crosstalk (e.g., several Gbit/s on a single line). Optical interconnections inside processors also eliminate ground-loop problems by isolating devices. Visual optics convey whole images with lenses in parallel, which is an operation that may not be very complex but involves enormous amounts of information. In imaging and other free-space optics, light from different points can cross freely within the system without difficulty, just as two light beams can pass through one another. This allows great topological freedom in interconnection. The following discussions show explicitly that optics is good for large numbers of low-complexity interconnections, including some very global interconnection patterns with large numbers of crossing lines.

Chip-to-chip bandwidth with conventional electronic packaging is currently limited to a few hundred channels. Reasons for this limit include topological constraints (bonding pads are situated at the edges of the chips), area requirements (size of the bonding pads and the driver electronics) and energy dissipation (for charging the bonding pad and the line). If optoelectronic interfaces are used as optical pins, as many as some 10 000 channels arranged in a two-dimensional array over the surface of the chip can communicate in parallel using imaging systems and the free space above the chip. The key physical problem with optics for communication inside processors is getting information into the form of light efficiently and easily. Much device research is devoted to reducing the operating energy of devices with optical outputs. The serious contenders for such devices utilize state-of-the-art technologies that, too, are the subject of basic research (e.g., molecular beam epitaxy).

Electrical interconnections in computers function relatively well for short distances inside chips, and can implement very complex interconnections. Because they are two-dimensional (albeit in multiple planes), these interconnections are subject to topological constraints. For long distances—either within chips, between chips, or between boards—electrical communication becomes progressively more expensive. Larger areas of the chip must be used to drive longer distances and, correspondingly, more power must be used. Large fractions of the chip area become occupied by the wiring rather than the logic devices. "Crosstalk" becomes increasingly troublesome at higher clock rates. The timing of the logic signals arriving at a gate from different parts of a circuit becomes critical. To avoid such "clock skew" problems, all interconnections within a complex system must be made equally long. The energy required to send a logic-level signal from one chip to another exceeds the logic switching energy of a single small electronic device by several orders of magnitude.

The problems of electrical interconnections have profound consequences for digital electronic systems. Com-

puter architects tend to minimize the communications off-chip wherever possible, leading to bus architectures with relatively few lines and hence to the classic Von Neumann bottleneck. This minimization also enhances the desire to put as much as possible on one chip. Ultrafast transistors with switching times of a few picoseconds have been reported. The system time constants for complex electronic digital circuits are, however, at least two orders of magnitude slower than those of the fastest transistors. System clock rate is dominated more by the time taken to communicate than by the speed of the fastest devices.

The physical root of the energy problem of electrical communication is the low impedance of free space. If we wish to send logic-level signals from one device to another, we are in practice constrained to charge up the entire line between the devices. Even if we send pulses down a lossless transmission line (such as a superconductor), we still have to charge a length of line that is as long as the pulse. The capacitance of lines decreases (and the impedance increases) as we increase the separation of the conductors, but only logarithmically once the conductors become separated by more than their lateral dimensions. Because of the low impedance of free space, we are stuck with low impedance lines (e.g., 50 Ω) and lines with high capacitance per unit length (~100 pF/m). Hence we cannot directly match small high-impedance logic devices to communicate logic levels over any long distance, and we must build large drivers.

Optics circumvents this by performing an effective impedance transformation [10]. Optical or optoelectronic devices can operate with internal logic levels of about 1 V (a visible photon has energy ~2 eV) even at very low power levels. Although the communication between one optical device and another is electromagnetic, it is not classical. Quantum sources or modulators and quantum detectors match the high impedances of small devices to the low impedances encountered in electromagnetic propagation. Therefore optical and optoelectronic devices do not need large line drivers. The switching energy of the device is also the communication energy and is essentially independent of distance. In optics the energy required is proportional to the area of the device. To minimize communication energy, we should use optics for all except possibly the shortest interconnections (e.g., ≤ 100 μm) [10].

III. Architecture

Digital optics will now be described, starting with all-optical architectures. In the first part of this section the architectural reasons for using optics within a processor are reviewed. Next, a specific approach, symbolic substitution, is discussed. In the third part another design approach—namely, one for programmable logic arrays (PLAs)—is described. Both approaches introduce parallel optical interconnections at the lowest possible computational grain size: they exploit the optical connectivity at the gate level. More conventional architectures could exploit optical interconnections before reaching the gate level; i.e., by using parallel chip-to-chip interconnections [4]. This hybrid optoelectronic approach will not be discussed in this paper. One should note, however, that the optoelectronic interfaces (section IV) and the parallel interconnections (section V) are immediately applicable for these hybrid systems.

A. Optical Architectures for Supercomputers

Conventional computers suffer from a bottleneck brought on by the limited number of interconnections that can be supported in a practical manner by electronics. This problem is referred to as the von Neumann bottleneck and involves the performance limitations imposed by the sequential and address-oriented communications between the CPU and memory in a conventional computer.

The source of this bottleneck can be found by examining the classical finite state machine, an ancestor of modern-day computers. The processor shown in Fig. 1 consists of

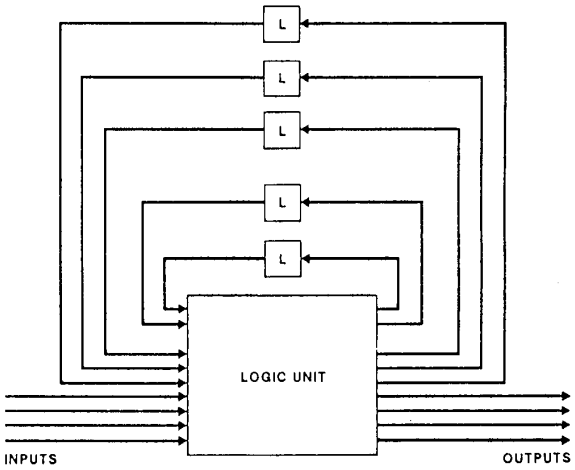

Fig. 1. Classical finite-state machine does not suffer from Von Neumann bottleneck.

storage elements, a combinatoric logic unit, inputs, outputs, and various interconnections. What is unusual about this processor is that it does not suffer from the von Neumann bottleneck. All the storage elements can be updated in parallel without the need for addresses. The bottleneck emerges when more storage variables are added. It becomes impractical to support large numbers of interconnections between the storage and logic units. As a result, the classical finite-state machine is modified to the structure shown in Fig. 2, in which a binary encoding scheme reduces the N interconnections from the output of the logic unit to the memory to $\log_2 N$ interconnections while a common return line reduces the interconnections between the memory elements and the input of the logic unit. This approach not only reduces the number of interconnections, it also degrades performance since the modified finite-state machine can address only one memory element at a time, and because an address is needed to specify which element. The interconnections are essentially time-multiplexed to compensate for the inability of electronics to implement N interconnections in parallel.

A similar constraint exists at the bus level of a computer. A processor is typically partitioned into boards. Ideally, each board is allowed to communicate with every other board. The impracticality of fully interconnecting M boards with $M \times (M-1)$ bus-wide interconnections leads to the use of a broadcast bus structure which trades time for a reduction in the number of interconnections. This results in the

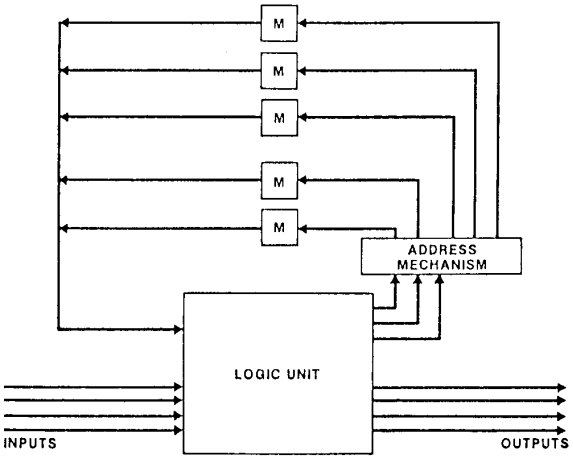

Fig. 2. Von Neumann bottleneck is introduced in modified finite state machine by using addressing mechanism in order to reduce number of interconnections.

sequential address-oriented communications characteristic of the von Neumann bottleneck.

A similar bottleneck occurs at an even lower level within a computer. Ideally, it would be nice if each bit of a memory chip could be independently read or written simultaneously. To accomplish this, a $P \times 1$ bit memory chip would need P input and P output lines. Since this is impractical, a binary encoding scheme is used to reduce the P inputs to $\log_2 P$. This approach is similar to that used in the modified finite-state machine and results in another sequential, address-oriented communications bottleneck.

These communications bottlenecks at the architectural, bus, and chip level all stem from the use of time multiplexing to compensate for an inability to effectively communicate N channels of information in parallel.

These problems carry over into software. The need to determine where to access every piece of data leads to additional computational overhead. The sharing of a common bus necessitates the introduction of contention resolution and queuing schemes. The limited bandwidth of the memory necessitates the use of cacheing.

Alternatives to the von Neumann architectures have been investigated, but these approaches still suffer from interconnection limitations. The single-instruction multiple data (SIMD) approaches rely on a broadcast approach and have the same problems as a shared bus approach. The multiple instruction multiple data (MIMD) approaches rely on an interconnection network. One such network that is commonly suggested is a crossbar. A crossbar is essentially a fully connected network, but its implementation is very awkward due to its N^2 growth. Other interconnection networks such as the hypercube and Clos-Benes network have also been suggested, but sacrifices in connectivity result in greater demands on routing and buffering.

The sacrifice in connectivity is complicated by the difficulty in exploiting parallelism. This search has led to smaller computational grain sizes, which necessitates more communication and internally requires more connectivity.

B. Symbolic Substitution

Symbolic substitution [11], [12] has been introduced as a method for performing optical logic by utilizing the parallelism of optics. It has been defined mathematically [13] and it allows parallel optical logic with limited fan-in and fan-out devices and with equidistant and space-invariant interconnections. The basic mechanism is to transform a binary matrix by applying several substitution rules in parallel. Every rule consists of a left side, determining the search pattern, and a right side, specifying the substitution pattern. A pattern is a spatial configuration of binary values.

The operation of a single substitution rule is best explained by Fig. 3. For simplicity we assume that the rule

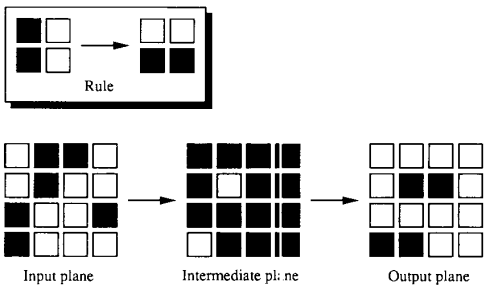

Fig. 3. Illustration of symbolic substitution: An input matrix is transformed according to given substitution rule.

consists of two dark cells on top of each other as the left side of the rule, and two dark cells next to each other as the right side. In the first step the occurrence of the search pattern in the input plane is marked in an intermediate plane. Thus the intermediate plane shows bright cells only at those locations, where the search pattern was found. In the second step, every white cell in the intermediate plane is replaced by the substitution pattern.

For the general case, the principle for recognition and substitution is outlined in Fig. 4. For each cell in the left side, the input matrix is replicated. To each of the copies k, a shift S_k is applied. The subsequent operation I_k is either an identity operation or an inversion depending on the state of cell k (dark or bright). In Fig. 4, all the I_k are identity operations. The shifted and inverted copies are superposed on a NOR-gate array, which inverts the input intensity, yielding dark cells wherever there were bright cells at the input. For the substitution, shown in the lower half of Fig. 4, the same steps as for the recognition are required. The input matrix is replicated according to the number n of cells in the right side of the rule. To each copy a shift S_k and an inversion I_k is applied. In the example, no inversion is necessary. The shifted copies are again superposed on the NOR-gate array. As a consequence of the identical operations necessary for recognition and substitution, the optical hardware for these operations is also the same. We will call such a split-shift-combine unit a dilation unit. There are two ways to look at the operation of one such dilation unit. If we focus at the input matrix, every input cell "sends" information "to" a certain neighborhood. If, however, we concentrate on the output matrix, we see that every cell at the output "receives" information "from" a certain neighborhood. Thus symbolic substitution can be considered as the minimal and most elementary shift-invariant array logic.

For the optical implementation of a recognition or a substitution unit there are two basic mechanisms. Additive logic, as described, superimposes shifted copies of the data

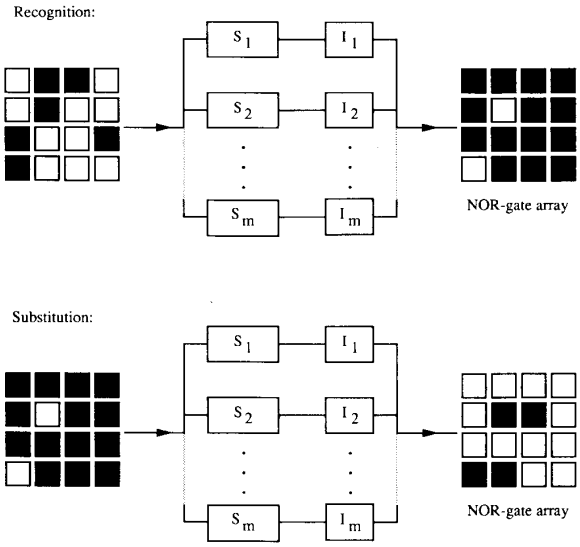

Fig. 4. Principle for realizing recognition and substitution. Top: Recognition. Input matrix is split into several channels. In each channel a shift and an identity or an inversion operation is performed. Combined output is superimposed on a NOR-gate array. Bottom: Substitution. Same operations are performed as in recognition stage.

plane and then applies a nonlinear operation to the intensity [12], [14]. For the generation of different copies, holographic beam splitters have also been suggested [15]. The use of correlation techniques to locate the searched pattern within the input plane [16] is also a method. The alternative method is multiplicative logic, which has been realized recently with spatial filtering [18]. A comparison of the performance of different optical implementations has been given in [17].

With symbolic substitution, logic is performed differently from conventional logic, where a physical mechanism acts on the input quantities producing an output state. Here logic is realized by substitution rules. Thus every possible logic function can be realized with the same hardware. Several rules are applied in parallel by processing the input matrix in several channels. Rules for the parallel addition of binary numbers were first given in [11]. Carry-free arithmetic operations in the residue number system have been implemented with symbolic substitution [19]. The "modified signed digit" (MSD) number representation also offers fully parallel carry-free operation, and rules for this kind of arithmetic have been suggested [20]. For binary image processing it has been shown [21] that morphological transformations can be implemented using symbolic substitution. By iteratively applying these operations, complex image-processing tasks, like edge extraction and feature suppression, can be achieved. Optical implementations of morphological operations have been given in [22].

The shift-invariant nature of substitution operations suggests that SIMD-operations are best suited to symbolic substitution. There are mechanisms to achieve also MIMD-type operations. One method is based on masking: by placing a mask in the intermediate plane, the recognition can be restricted to certain locations in the matrix. Another method is based on combining the data with control information (Fig. 5). Different cells in the input matrix contain information from the control and the data array. The substitution

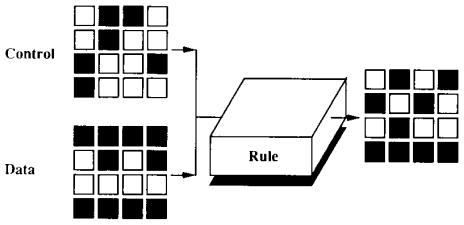

Fig. 5. Combining data array with control array to achieve MIMD operations.

rules acting on the combined information produce different results depending on the control cells, thus allowing MIMD-operations although the hardware is shift invariant. A processor based on this mechanism was suggested in [23].

C. Optical Circuit Design with Global Interconnections

Symbolic substitution allows the design of digital optical circuits making strict use of regular (space-invariant) interconnections by imaging between two-dimensional arrays of optical logic gates. For complicated circuits, interconnection patterns that allow global data communication across the gate array are desirable. We discuss an architecture that incorporates global interconnections, such as the perfect shuffle, the banyan or the crossover, between the gate arrays. Fig. 6 shows the conceptual layout (see also [24]). The optical logic devices on an array are arranged at the crosspoints of a grid, perform identical logic operations at each site on the array, and have an identical fan-in and fan-out of at least two. The absolute minimal requirements on the performance of the logic devices are made [50]. During the communication, the data is permuted as specified by a global interconnection pattern. Masks are inserted in the image planes to customize the circuitry by blocking light at selected locations.

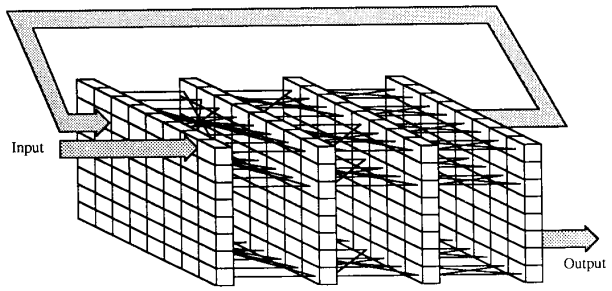

Fig. 6. Arrays of optical logic gates are interconnected with crossover.

The main addition compared with symbolic substitution logic are global interconnections, such as the perfect shuffle, the banyan, or the crossover. These three interconnections hold an isomorphic relationship with each other. They can be mapped onto each other by replacing one interconnect with another and appropriately relabeling the nodes. This procedure is illustrated in Fig. 7. Hence architecturally these interconnects are equivalent. For the purpose of consistency the banyan will be used throughout this section to illustrate our ideas.

"Programmable logic arrays" (PLAs) can be designed with banyans [24] interconnecting gate arrays such that the same order of complexity growth for circuit depth and width is maintained that might otherwise be achieved with more arbitrary interconnection schemes. Further compaction of the circuit can be achieved by manually optimizing the connections [25]. A layout for a parallel random-access memory (RAM) that achieves a hardware complexity of between one and two switching components per stored bit of information has been described [26].

To illustrate the principle, we show the design of a finite-state machine which serves as a sorting node for a self-routing switching network. The design is based on a shuffle-exchange network that consists of alternating layers of perfect shuffles and arrays of serial sorting nodes. Each node either transmits or exchanges two adjacent channels. The function of each node is locally determined from the incoming data ("self-routing"). The sorting is based on Batcher's bitonic sorter [27]. A VLSI implementation of the node has been created at AT&T Bell Laboratories for the Starlite Wideband Digital Switch [28]. It requires 106 switching components. The optical design uses a comparable number of switching components (about 128) even though the gate-level interconnects are restricted to a regular pattern.

The finite-state machine for the switching node has three internal states: the incoming data are transmitted through the node either in a straightforward manner (bypass state) or they get swapped (exchange state) or the node is undecided. It is a standard procedure in computer science to express the function of the node as a set of Boolean equations [24]. These equations depend on the two data inputs x and y and on the previous state of the node expressed by the state variables s_0 and s_1. The functions f_0 and f_1 describe the next state of the node, and f_2 and f_3 are the sorted outputs:

$$f_0(s_0, s_1, x, y) = s_0 + \bar{s}_1\bar{x}y \tag{1}$$

$$f_1(s_0, s_1, x, y) = s_1 + \bar{s}_0x\bar{y} \tag{2}$$

$$f_2(s_0, s_1, x, y) = s_0x + s_1y + xy \tag{3}$$

$$f_3(s_0, s_1, x, y) = \bar{s}_1\bar{x}y + \bar{s}_0x\bar{y} + xy. \tag{4}$$

These functions are implemented as optical PLAs. The layout is done in two parts [24], one for the top half of the PLA (the AND stage, where all the necessary AND-operations are performed) and one for the bottom half (the OR stage, where the results from the AND-stage are combined). A possible layout for the AND stage of a PLA is shown in Fig. 8. The layout is obtained either by computer utilizing algorithmic design techniques [24] or by hand-utilizing a semiautomatic trial-and-error approach. A layout for the OR stage looks, in principle, quite similar; the difference between the AND stage shown in Fig. 8 and the OR stage is that all the gates are OR-gates and that different data paths are masked out.

Conventional digital circuits can be created with little

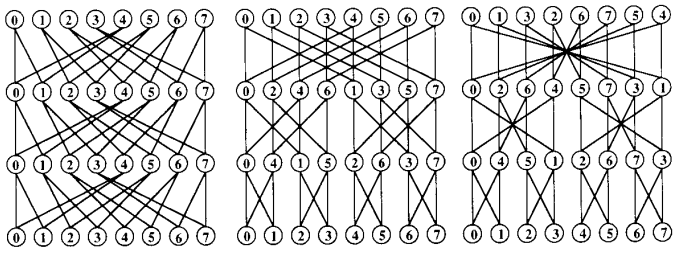

Fig. 7. Comparison of communications capabilities. (a) Perfect shuffle. (b) Banyan. (c) Crossover interconnection network. All three are topologically equivalent if nodes are relabeled appropriately.

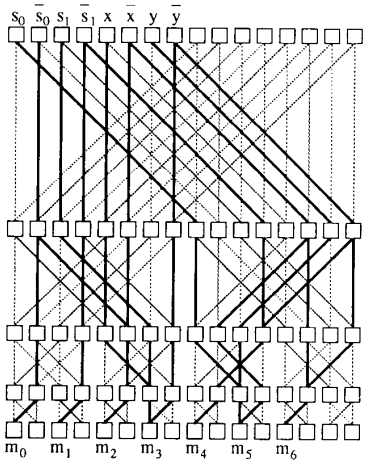

Fig. 8. Connection diagram corresponding to AND stage of AND–OR PLA for implementation of self-routing switching node. Dimmed connections are masked in image planes. All logic gates are AND.

additional hardware complexity when constraints must be adhered to, such as regular interconnects at the gate level, identical logic functions at each level of circuit depth, and fan-in and fan-out of two. The forced regularity does more than just allowing the use of free-space optical interconnects. For example, it is possible to create setups that provide an equal pathlength for every signal. This reduces signal skew to a negligible level because signals are regenerated at each stage. Circuits can therefore be pipelined at the gate level, they can maintain a throughput that is limited only by the switching speed of the devices, and pulsed logic can be used. Furthermore, free space may be used as a form of serial storage or a delay line memory [26].

IV. Optoelectronic Interfaces and Optical Logic

In the following section the nonlinear devices for digital optics will be discussed. First we address optoelectronic devices. They can be used as interfaces from electronics to optics for interchip connections, or they can be run as optical logic gates in an all-optical architecture. In both cases electronics is used only for short-range communication. Secondly, all-optical devices based on microresonators are described. They offer the potential for low-energy all-optical processing. In the third part, the light sources for digital optics for discussed.

A. Optoelectronic Devices

It is easy to conceive of optoelectronic devices capable of performing the basic logical functions for computing. For example, we could propose some simple circuit with phototransistors as input devices and a light-emitting diode or laser diode as the output device. There are, however, two key problems: one is integration and the other is energy. Both of these problems arise because we wish to use devices in reasonably large digital systems. Large numbers of devices mandate integration for cost, reliability, and manufacturability. Energy dissipation and the associated power supplied are obvious constraints, especially for the case of optical power supplies. Light-emitting diodes are not efficient sources of usable photons although they are easy to make and may be usable if we have optical devices requiring very low input energies [29], [30]. Laser diodes, although they are probably the most efficient light source available, are not generally very efficient at low powers. Furthermore, laser diodes are very demanding in fabrication; the process must usually be highly optimized for the laser diode, making integration with other components difficult. At this time also, nearly all laser diodes are waveguide devices; true "surface emitting" diodes are still in early research stages. Thresholds for laser diodes are being reduced [31] and such devices are an interesting option for small numbers of high-speed optical-fiber interconnections between chips and boards. It is also possible to make logic devices based on the laser diodes themselves [32], although these suffer the same integration and power problems in large systems.

A new option that has recently emerged is the quantum-well self-electrooptic effect device (SEED) [33]. Quantum wells are semiconductor structures made of alternating very thin layers (e.g., ~ 100 Å) of two different semiconductors, typically gallium arsenide (GaAs) and gallium aluminum arsenide (GaAlAs). These structures have an unusually large electroabsorptive effect; that is, they can be changed from opaque to transparent by applying a voltage to them. This mechanism is called the quantum-confined Stark effect. A typical structure utilizing this effect to modulate a light beam is shown in Fig. 9. The quantum wells consisting of

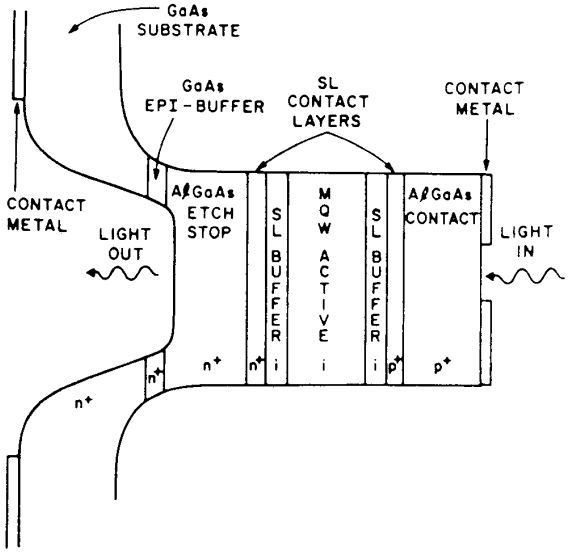

Fig. 9. Schematic illustration of quantum well optical modulator. Superlattice buffers around multiple quantum well region are optional. Whole structure may be ~ 4 μm thick.

~ 100 layers of total thickness ~ 1 μm are contained within an undoped region in the middle of a diode. The diode is reverse-biased to modulate the transmission of a light beam. Typical operating voltages are ~ 5–10 V, with devices of a few microns total thickness. This will change the transmission of the light beam by a factor of 2–3. Such structures are typically grown by molecular-beam epitaxy on GaAs substrates. An integral mirror, also made out of layers of

GaAs and GaAlAs, can be grown under the diode to give a reflecting device [34].

The concept of the SEED is to combine such a quantum-well optical modulator with a photodetector so that light shining on the photodetector changes the voltage across the quantum-well diode, giving a device with optical inputs and outputs. Such a device does not generate light; instead the concept is to generate many light beams from one efficient high-power external laser diode, and to modulate them with the quantum wells. Importantly, the SEEDs can work efficiently at low powers and can be integrated.

Fig. 10 illustrates the symmetric SEED (S-SEED) [35], a simple bistable SEED that nonetheless is actually an effective

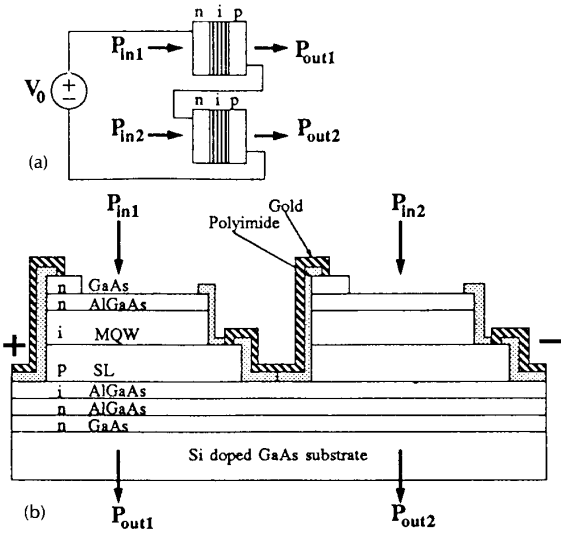

Fig. 10. Schematic diagram. (a) Symmetric SEED circuit. (b) Symmetric SEED structure.

three-terminal device. In this device, there are two quantum-well diodes in series with a reverse-bias supply. Both diodes function simultaneously as modulators and photodetectors. In one stable state, the left diode is highly absorbing and the right diode has all the bias voltage across it. As we increase the power into the right diode, it eventually starts to generate more photocurrent than the left diode, and the voltage across it starts reducing. This reduction increases the absorption in the right diode and decreases the absorption in the left diode, further increasing the difference in currents, leading to switching and bistability. This device can be set in a stable state with low power, and read out at high power, giving usable gain in a clocked system. It can operate as a latching logic gate. Because of its simplicity, it is easily integrated. 16 × 8 arrays of fully functional devices have been demonstrated [36]. With the use of 256 light beams, all of these devices have been operated simultaneously.

SEEDs can also incorporate transistors for more functionality. Laboratory demonstrations have been made of a field-effect transistor SEED [37] (F-SEED). Here, field-effect transistors (FETs) are fabricated directly in the top layer of the modulator structure. As the drain voltage of the FETs alter, so also does the voltage over the modulator directly beside and underneath the drain. Thus we can have an optical "output pad" beside every desired FET in the circuit. Importantly, such "pads" need not be large e.g., 5 × 5 μm, and can exploit the optical impedance conversion discussed in section II. It is also possible to use the same diode structure elsewhere as a photodetector, thus allowing optical inputs. Fig. 11 shows the simple case of an optical signal

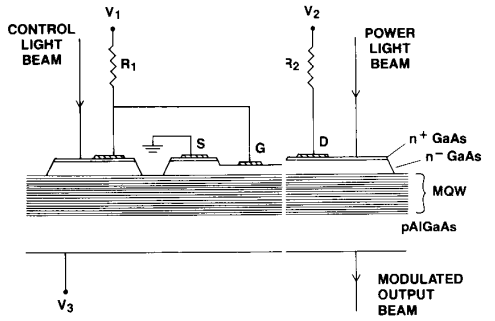

Fig. 11. Schematic of field effect transistor SEED (F-SEED) showing MESFET fabricated in top layer of quantum well modulator/detector diode.

amplifier; however, more complex logical functionalities could be implemented with more devices. This concept is compatible with standard metal-semiconductor FET (MESFET) processing.

SEEDs are well suited for relatively large digital systems because they are integrable low-energy devices. Operating energy densities are comparable to electronics (e.g., 1–20 fJ/μm^2) and are very low by optical device standards. The devices operate at room temperature, although some temperature stabilization (e.g., ±2 K) relative to the laser source will probably be required to maintain optimum operation at the correct wavelength. They are compatible with electronics and with laser diodes. They can operate at speeds comparable to electronics: the internal speed limitations are similar to electronic devices because carrier transport and charging of the device are involved. Subnanosecond switching times and picojoule energy dissipation per switching event have been experimentally demonstrated. The ability to integrate two-dimensional arrays with functional electronic devices means that we may choose where we wish to make the break between optics and electronics, perhaps to get the best of both worlds. At the time of writing, there are encouraging indications that these devices could also be grown on silicon substrates [38], [39], perhaps in conjugation with silicon electronics. If so, this would open up many exciting opportunities for hybrid digital optics.

B. Semiconductor Microresonator Devics

Optical resonators (Fabry–Perot etalons) form the basic structure for many optical logic devices, also for lasers. Resonator-based optically bistable devices and optical logic gates have been investigated intensively [3]. To reduce the operating energy and the switching speed it is important to scale these structures (as well as any other type of device) to sizes as small as possible.

The use of "ion-beam-assisted etching" to form ~1.5-μm diameter waveguiding "posts," or microresonators, in a GaAs/AlAs Fabry–Perot structure grown entirely by molec-

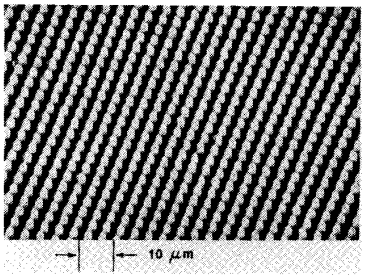

Fig. 12. Scanning electron micrograph of small portion of array of microresonators.

ular-beam epitaxy (MBE) has reduced the device's cross-sectional areas, energy requirements, and recovery times, all by more than an order of magnitude [40]. Fig. 12 shows a small region of the etched heterostructure. Prior to etching, the minimum controlling energy required for an optical logic etalon operation [41] was 20 pJ. The device diameter, defined as the illuminated region, was about 10 μm, and recovery time was estimated to be several nanoseconds, both inferred from measurements on comparable devices. For 1.5-μm microresonators, the energy is 0.6 pJ, and recovery time ~200 ps. Thus, at least over this size range, the energy and time requirements scale directly with area.

It is possible that this scaling down will continue to approximately λ/n diameters (λ being the wavelength of light and n the refractive index of the semiconductor), i.e., to ~ 1/4 μm for GaAs, or a factor ~ 36 reduction in area. This would reduce controlling energies to ~ 17 fJ and recovery times to ~ 6 ps for the same Fabry-Perot design. Experiments on gating in a ~ 0.5-μm diameter device yielded a ~ 30 ps recovery, in agreement with our expectations [42]. The energy requirements could not be tested fairly since the transmission peak was at 8575 Å and the pump beam was not focused as well as the probe. Still, a small fraction of the 3 pJ pump pulse produced 75 percent modulation by saturating the bulk GaAs well into its absorption band (Fig. 13). Such small waveguiding etalons also exhibit waveguide dispersion, which causes the transmission peak wavelength to vary with the microresonator diameter [42].

The energies (but not recovery times) can be much further reduced by use of thinner higher-finesse etalons [43]. Recently we have achieved optically pumped lasing in a very-high-finesse structure containing only a single quantum well as the active material [44]. The absorbed energy density in our room-temperature experiments was ~ 12 fJ/μm^2 for pulsed operation and ~ 7 μW/μm^2 for continuous wave (CW) pumping. Since optical gating typically requires 10–15 times less energy than optically pumped lasing, these results indicate that gating in a 0.5-μm device could be achieved with less than 1000 photons if scattering losses do not degrade the finesse too much. Alternatively, a system can be envisioned which would have electronic detectors whose signals, when amplified, could drive electrically driven microlasers. Although the power requirements would be larger than for the all-optical case, this kind of system would be much more robust to imperfections in device uniformity and optical alignment of the beams. Furthermore, it could be simpler and more compact since there would no longer be the need for large external lasers, array generators, and many of the beamsplitter/combiners. At this point it is worthwhile to investigate microresonators both as all-optical gates and as electrically pumped lasers. The latter could also be useful for chip-to-chip communication.

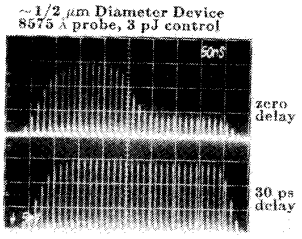

Fig. 13. Pump and probe data from smallest (~ 0.5 μm) device. Top trace: Envelope of reflected 8575 A probe pulses without pump (left side) and with pump (right side). Thus pump pulses switch resonator from high to low reflectance. The ~ 100 ns slopes are characteristic of the acoustooptic modulators, not of the devices. Bottom trace: Same as upper but with 30 ps relative delay of probe pulses. Recovery is nearly complete.

Coupling light into (or out of) such small devices requires lenses of very high numerical aperture (NA). The full width (from zero-to-zero intensity) of the central lobe of an Airy disk from a uniformly illuminated lens is about 1.2 × λ/NA. Lenses for compact-disk players (such as the one used in our experiments) typically have NA ~ 0.5, yielding a spot diameter of ~ 2 μm for λ = 0.89 μm. Thus, with these lenses, even the 1.5-μm devices are losing some light due to insufficient focusing power. Since it is not feasible to increase the focusing angle significantly (for large arrays of devices), we instead increase the NA by focusing through a high refractive index medium. This reduces the diameter by a factor equal to the refractive index. Using a NA = 0.55 lens focused through a hemisphere of $SrTiO_3$ with n = 2.4, we achieve NA = 1.3 and focus to a full diameter of only ~ 0.7 μm. Use of a semiconductor with $n > 3$ allows focusing to < 0.6 μm and device diameters ~ 0.5 μm [42]. The devices can be grown on a transparent semiconductor substrate with lens surfaces formed on the backside by a nonlabor-intensive process such as photoelectrochemical etching [45]. The single quantum well in the laser just described was an 80-Å well of $In_{0.2}Ga_{0.8}As$, and the lasing wavelength was 980 nm where the GaAs substrate was transparent. Microlenslets with diameters ~ 200 μm have been etched in InP wafers, and the process is extendable to GaAs. Thus many of the prerequisites for systems of submicron low-energy devices interconnected by microoptics have been demonstrated.

At ~ 1-μm wavelength it is impractical to focus to much smaller than ~ 0.5-μm beam diameters over many devices. The devices themselves may be somewhat smaller since the waveguide intensity profile will have some power outside the guide. If even smaller diameters are desired, there is still an option: tapering the waveguiding devices. Such a device would resemble a microwave horn. Preliminary experiments using microwaves and dielectric tapered waveguides suggest that the necessary tapering in GaAs optical waveguides might be accomplished over a length of only about 2 μm. If light needs to be coupled into and out of only one side of the device, then only that side needs the "optical horn." Optical horns might be formed by varying the etch parameters during etching.

With the achievements made in microresonator devices and the improvements suggested, we expect to reduce the gate-controlling energies to <1 femtojoule, approaching the statistical limit for reliable switching of a few hundred photons [46], [47]. Recovery times should be around 10 ps. Energies required to achieve lasing should also be in the range of a few fJ, making them well-suited for optical chip-to-chip communication and viable candidates for switching/gating devices.

C. Optical Power Supply

The devices which are currently available for use in optical digital computers place several severe restrictions on the optical power supply used. Different devices need optical power in either sharp pulses of light, as is required by the optical logic etalons, or as quasi-continuous waves of light, as is required by the various SEED-type devices (in this case, the laser emits rectangular clock pulses). There are several advantages in using such a pulsed operation inside an optical computer. First, free-space optical interconnections used in conjunction with pulsed logic offer the possibility of running a computer with little effect of clock skew since all the outputs of the devices would be read at the same time. No additional latching is necessary for synchronization. Clock skew is one of the major engineering considerations in today's fastest electronic computers. Optical interconnections can be made equal in length down to subpicosecond accuracy. Secondly, free-space might be used as a transient memory since images of information can be propagated from one logic module to the next with several images stacked in between the successive modules [26]. For example, if the modules were placed 1 m apart in a computer with a clock rate of 1 GHz, three images of information could be propagated simultaneously between the two modules.

The requirements placed on the optical power supply are determined by the speed, number, and energy requirements of the devices. What is presented here is a best estimate of what will be necessary for a competitive first-generation computer. A repetition rate (or clock rate) of at least 1 GHz is required to compete with electronic computers. Devices currently available require energies in the picojoule range [35], [36], [44]. Ten thousand optical devices on a single two-dimensional matrix of devices is a realistic first step given the limitations of device fabrication and the optical system design. To preserve the temporal and spectral synchronism between all of the pixels, it is assumed that all 10 000 pixels are generated using a multiple beam splitter [48], [49], [53] with power supplied from a single laser source. Taken together, this places a lower limit on the laser source of 10 W of average power at a 1-GHz repetition rate for each individual logic module.

There are several characteristics of the laser source, in addition to the average power and repetition rate, which are also required. Since the energy for performing a logic operation is linearly related to the spot size or switching area, the beam quality of the source laser must be Gaussian and diffraction-limited such that it can be focused to spots with as small diameters as possible. To synchronize the optical power supply output to both itself and power supplies for other logic modules, the repetition rate variation and phase noise must be kept to a minimum which is feasible for certain types of lasers [53]–[57]. Any variation would incur clock skew. The wavelength tolerances associated with today's devices (particularly with the microresonator devices) are quite stringent, both in the actual wavelength and in the spectral stability [44]. For the GaAs-based devices this wavelength is around 850 nm with a width of 1 nm. In addition to the spectral stability the amplitude stability must be quite good to ensure that the devices always switch [50]–[52].

It is unreasonable to consider a large flashlamp pumped laser as the power source for each individual logic module in an optical digital computer. Where continuous-wave lasers are required, laser-diode arrays will be used since they can now produce high average powers at the wavelengths that the GaAs based devices are operating. Problems associated with the focusability, operating wavelength, and stability should be resolvable. In pulsed-mode computers the power source most likely will be a laser-diode-pumped mode-locked solid-state laser since the laser diodes themselves will be damaged if used in pulsed operation. The prospects for being able to provide the power required for optical digital computing are promising in the long run.

V. Optical Systems for Interconnection

Architectures and switching devices for digital optics have been introduced in the preceeding sections. Now we concentrate on free-space optical interconnections. First, global interconnection systems are described. The splitting and joining of data paths is a key operation in digital optics. Light-efficient data joins are discussed in the second paragraph. In the third part of this section, packaging of complex optical systems is addressed.

A. Imaging Systems for Interconnection

Much has already been said in favor of optical free-space interconnections by imaging systems (section II). At the core of the architectures (section II), we have regular two-dimensional arrays of logic gates. The input signals to these gate arrays are provided by imaging previous gate arrays onto them. The shuffle-type interconnections, which allow global data permutations and which are necessary for architectures such as those described in section III-C, will be discussed next.

In section IV it was argued that practical optical-logic gate arrays are necessarily small to reduce the cycle time and the energy dissipation. This means that the imaging lenses must have high numerical apertures. At the same time we want to run many devices on an array in parallel. The devices might not be densely packed, since some space is needed to avoid optical or thermal crosstalk (and to bring in the electrical power in case of the SEEDs). Part of this "dead space" between the devices can be recovered by putting lenslet arrays with large aperture on top of the device arrays, with one focal length spacing. Then the external imaging system needs to focus only on the lenslet and not on the devices themselves. In any case the imaging lenses, as well as all other optical components (such as beam splitters etc.), must have a reasonably large "space bandwidth product" (resolution and field of view). With custom designed optics it should be possible to run on the order of 100×100 devices on one chip in parallel. Larger arrays place stringent demands on optical systems. In that case, multichannel

imaging systems using two-dimensional arrays of lenses might be a way to increase the field.

Global optical interconnections that allow long range communication within a data array are architecturally desirable. Perfect shuffles, banyans, and crossovers allow arbitrary data communication in logarithmic time. Several optical implementations for the shuffle, banyan, and crossover have been proposed and experimentally realized [2], [24], [58]–[64]. Since these interconnection patterns are topologically equivalent, the problem of which one to implement depends on practical reasons. At the core of all implementations lies one important realization, namely that the interconnection patterns are quasi-regular. All three interconnects can be decomposed into three steps. First, the input data array is split into several parts. The three interconnects differ in the second step, where different operations are applied to the copies of the input plane: in the case of the perfect shuffle there is a magnification of 2 applied to the data paths. In the case of the banyan, the data paths remain as they are, except that they are shifted in respect to each other. In the case of the crossover, one of the two data paths is inverted, that is, the sequence of the data channels is reversed. Operations such as magnification, shifting, or inversion can be easily implemented with classical optics. The third step in performing a global interconnection step is the recombination of the data paths with an appropriate interleave. The joining of different optical channels will be discussed in the next paragraph. Joins are needed to combine information-carrying beams as well as the energy-carrying power-supply beams.

B. Splitting and Combining Beam Arrays

At the current stage most systems experiments are tailored towards modulator-type devices such as the SEED. Therefore, on the gate array, several arrays of optical beams must be combined. One array of optical beams must be produced from a single-power-supply laser, each beam having the same intensity. These beams serve as read-out beams for the logical state of the modulator. In addition, these beams are used to clock the system since they are generated from a pulsed or modulated laser source. We will call this the power supply array. Our initial solution for generating a multitude of power supply beams out of one high-power laser is the use of a multiple-beam-splitting device based on light-efficient binary-phase gratings [48], [49]. Secondly, at least two input-beam arrays (for devices with a fan-in of two) that carry the information from previous gate arrays must be provided to the switch array. Third, the output beams (i.e., the power supply beams that have been modulated by the switch) must be taken out from the array. This is especially difficult for the reflection-type devices. Unfortunately, reflective devices are being preferred to transmission-type devices since they allow cooling from the back side. In reflection, the output occurs at the same side as the input and it must be separated from the other beam arrays. The output array is put through an interconnect such as a shuffle, banyan, or crossover. Some unwanted outputs may be removed by absorbing masks that are determined by the design (section III-C). For devices with a fan-out of two, the resulting arrays must be split into two branches. The resulting arrays contain the input information for the next logic stages.

The problem we concentrate on is having the array of logic gates in the focal plane of a single lens and feeding our array of power-supply beams plus our arrays of input beams onto the array of devices without losing power or sacrificing the resolution of the lens (which would mean we require larger devices and hence more power [50]–[52]). Each individual signal or power supply must use, as near as possible, the whole aperture of the lens so that the resolution is not reduced. Another constraint we have set is that we never want to have two beams of the same polarization overlapping on the same position on a device. The reason is that if two such beams overlap, the whole system must be set up to interferometric precision or else interference will result in spurious signals. Guaranteeing interferometric precision throughout a complex system consisting of a large number of modules seems impractical to us.

Several methods can be used to achieve the aforementioned goals, and we want to illustrate the ideas by describing one approach in more detail: the beam combination based on polarization and "patterned reflectors." The simplest way to combine arrays of beams without loss is to use polarization. Using a polarizing beam splitter, two orthogonally polarized arrays of beams can be combined or separated. There are, however, only two orthogonal polarizations, so this method is limited to splitting (or joining) two signals only.

A simple method to combine two arrays onto the same polarization without power or resolution loss is shown in Fig. 14. The necessary optical elements are a polarizing

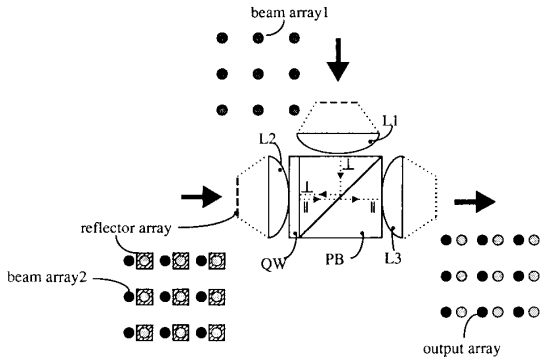

Fig. 14. Method for space-multiplexing arrays of beams with no power or resolution loss.

beamsplitter (PB), a quarter-wave retardation plate, several lenses (L1, L2, and L3), and an array of patterned reflectors. The array of beams (beam array 1) is arranged to be vertically linearly polarized ("s-polarized"). The beams are collimated by lens L1 and are reflected by the polarizing beam splitter (PB). They then pass through the quarter-wave plate (QW) and are circularly polarized. This array of beams is focused by lens L2 into an array of spots at the plane of the reflector array. The reflector array's position, spacing, and size is such that the spots are incident on it and are reflected back through L2 and QW. Now the beams are horizontally linearly polarized ("p-polarized") and are so transmitted through the beam splitter. L3 focuses the array into an array of spots.

Beam array 2 is incident from the right and circularly polarized. This array is arranged so that it is focused to an array of spots in the reflector plane, but the positioning is

such that the spots are transmitted between the reflecting patches of the reflector array and collimated by L2. The polarization is such that the passing through QW it is converted to p-polarization, and so is transmitted at PB. Thus the output array consists of the two input arrays "interlaced" and in the same polarization. This method can be used to "space multiplex" many arrays of beams together without losing power or resolution, in principle.

This approach has been used to construct compact easy-to-align optical interconnect modules both for optical computing [65] and for optical interconnect [66]. A modular implementation of an optical logic module using an array of 21 symmetric self-electrooptic-effect devices (s-SEEDs) has been built and tested [67].

C. Planar Packaging of Optical Components

One of the main questions when building optical circuits is: How do we put all the components together with a submicron precision so as to ensure stability despite influences such as temperature changes, mechanical stresses, aging effects, etc? The optics must be aligned relative to the device arrays with a precision that is given by the size of an individual logic gate in the array. The size of one individual logic gate is probably going to be a few microns, maybe less. This means that the alignment of the optical components must be done with a "submicron tolerance." Conventional mechanical mounting allows only for a precision typically in the range of 10 μm. Precision alignment stages can go one order of magnitude farther down in scale, but only by increasing the expense dramatically. Futhermore, for real-world applications we need to be able to build robust and cost-efficient systems. Therefore it makes no sense to have micrometer adjustment stages attached to each of the optical components in our system.

Rather than building systems out of many individual components mounted mechanically, we must find ways of fabricating and packaging free-space optical components in an integrated fashion. The goal is to reduce the number of mechanical degrees of freedom. This may sound trivial, but it is actually the lesson that was taught by microelectronics. Electronic systems became cheap and reliable only after the integration of devices and interconnections into compact modules with standardized interfaces. For free-space optics, this means finding new ways of fabricating and designing optical systems.

To find an economic method of fabricating integrated free-space optical systems, we must use fabrication techniques similar to those used in VLSI. There are planar technologies such as pattern generation by an electron beam writer, lithography, etching or material deposition, etc. An electron beam writer can generate geometrical patterns with a positioning accuracy on the range of 0.1 μm and a feature size of 1 μm or less. This allows the placement of patterns on a planar mask that can be several inches in size. Such a mask can be used to fabricate optical components that are based on light diffraction or refraction using subsequent steps like reactive ion etching.

Lithographic techniques have already been employed during recent years to fabricate individual optical components such as lenses or beamsplitters [68]-[73]. The basic steps required for the fabrication of a diffractive optical element using e-beam lithography and reactive ion etching are

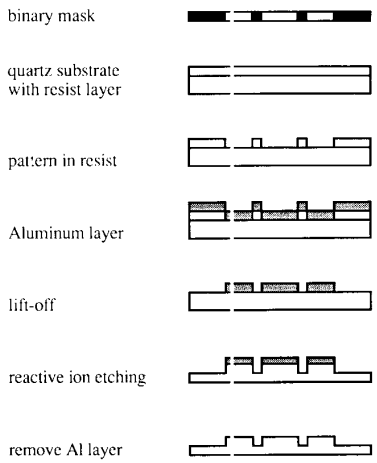

Fig. 15. Fabrication of phase grating using lithography and reactive ion etching. Pattern is generated by electron-beam writer or laser writer under computer control.

shown in Fig. 15. For any optical system, we need components such as lenses and beamsplitters. Using planar techniques it is possible to fabricate these based on either refraction, reflection, or diffraction. The approach based on diffraction is probably the most unconventional, although it is not new. A diffractive lens, for example, can be made by using Fresnel zone patterns (FZPs). A high efficiency is obtained by implementing the FZPs as blazed phase structures with multiple discrete phase steps. The more phase levels used, the higher the light efficiency. For a diffractive lens with eight phase levels (Fig. 16), the theoretical value

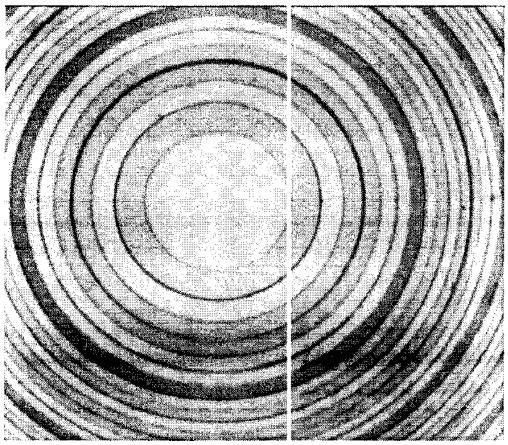

Fig. 16. Top view of diffractive lens with eight discrete phase levels.

for the efficiency is 95 percent. Beam splitters that split a single beam of light into two or more can be generated by computer techniques and fabricated in the same way as it was described in the preceding. Special beamsplitters that generate two-dimensional arrays of spots were proposed by Dammann *et al.* [48], [49], [74]. They are useful for producing power-supply beam arrays.

Now that we have discussed one method (out of several) for the fabrication of individual optical components using

planar technology, we can consider how to build more complex systems using that concept. To this end, we consider a specific example. Fig. 17 shows a typical optical-imaging setup consisting of an input object, two lenses, and

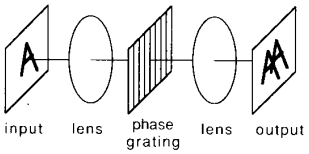

Fig. 17. Optical imaging setup.

a spatial filter between the lenses. The setup shown could be used, for example, to implement the split-and-shift operation needed for symbolic substitution, or for a shuffle or banyan interconnection. In this case a binary-phase grating is used as a spatial filter which basically generates two shifted copies of the input object in the output plane. We want to implement the same setup in a planar way. Fig. 18

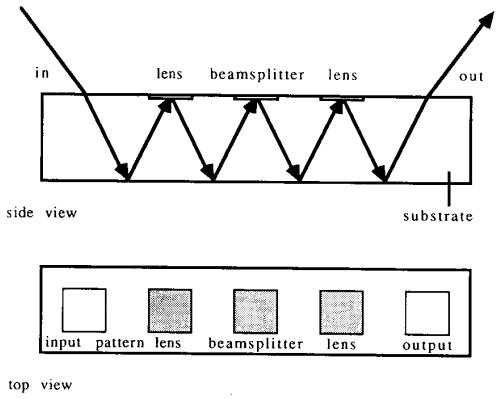

Fig. 18. Planar implementation of setup shown in Fig. 17. Light travels in glass substrate along zigzag path. Both sides of substrate are assumed to be reflective except for input and output window.

shows how the components must be arranged to achieve this goal. The main idea is that now the light follows a zigzag path between the two sides of a quartz glass substrate for example. The optical components, i.e., the two lenses and the beamsplitter, are placed on one or two sides of the substrate. To minimize alignment problems, it would be an advantage to put all alignment critical components on one side only. The simplest example for such a situation is shown in the figure, where the lower side of the substrate is assumed to be mirrored or the angles large enough for total internal reflection. Similar multimode waveguide approaches have been proposed in the context of holographic optical interconnections [75], [76].

The advantage of such an integration of optical components is obvious: rather than dealing with many individual components that must be aligned in three spatial and three angular coordinates each, we now have one piece of glass with less mechanical degrees of freedom. In Fig. 18, only the basic idea of integrating free-space optical components in a planar way is described. A large number of variations are possible but cannot be discussed here. A more comprehensive description is given in [77]. One extension of these ideas deals with the combination of several modules: we can use the same techniques as are used for the fabrication of the optical components to mount two modules. A number of grooves can be etched into two substrates in such a way that they fit together precisely. (Fig. 19). Index-matching might be used to avoid reflections and

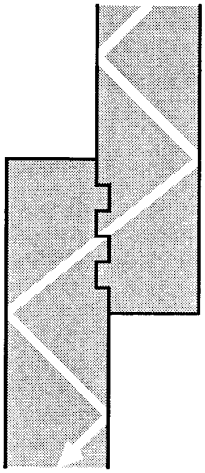

Fig. 19. Two modules with planar optical components can be mounted together by using grooves which are etched into substrates.

scattering when the light passes from one module to the next. Our approach also has some limitations when compared to conventional optical components. A diffractive lens may not reach the imaging quality and field size of a camera or a microscope lens which actually consists of a group of individual lenses. This may suggest hybrid approaches with combinations of conventional and diffractive components in the spirit of "stacked planar optics" proposed by Iga [5], [70]. To solve the packaging and adjustment problems, planar integration of free-space optical components seems to be a viable and necessary approach.

VI. Conclusion

In our survey, we focused on one specific approach of digital optics, based on free-space optical-array interconnections. We discussed the interdisciplinary issues, such as the properties of optical architectures, logic gate arrays, light sources, and free-space interconnections.

Microelectronics is the technology at the base of digital computing, digital communications, and of a few other information processing activities. Similarly, digital optics may well evolve into a technology of comparable significance. Optical communication via fibers, optical memories, and optical sensors would benefit directly from digital optics technology. Digital optics should not be viewed only as a competition to microelectronics. On the contrary, we expect progress due to hybrid approaches [4], [67] and cross-fertilization.

Optics can be used in an information processing system on different levels of hierarchy. For example, in a self-rout-

ing switch for telecommunications, the sorting node could be implemented optically on the gate level (as discribed in section III-C). Alternatively, arrays of sorting nodes could be built on VLSI chips with optoelectronic devices as input and output pins. Then optics would be utilized for interconnecting electronic processing "islands." One would still profit from the global and low-energy interconnection capabilities of optics, but the complexity of the data processing would remain in the realm of microelectronics.

In telecommunications, the switch fabric within a switching system is probably the first candidate for an optical circuit that is competitive with electronics. In the switch fabric, several hundred parallel high-bit rate signals must be sorted and sent to their final destinations. This problem is well suited for an optical implementation because it demands high parallelism, high throughput, and because it may be pipelined at the gate-level.

Applications to supercomputing are the next logical step. A switching network is directly useful for routing information between multiprocessors and shared memories. Any kind of pipeline problems, such as signal-processing, are well suited for an optical implementation. Other problems require a major redesign of the architecture whereby advanced design strategies, such as "computational origami" [78], will prove useful.

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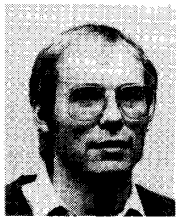

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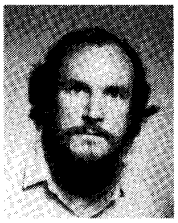

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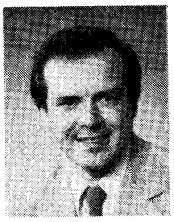

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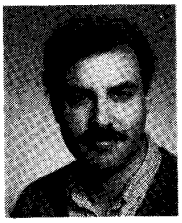

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